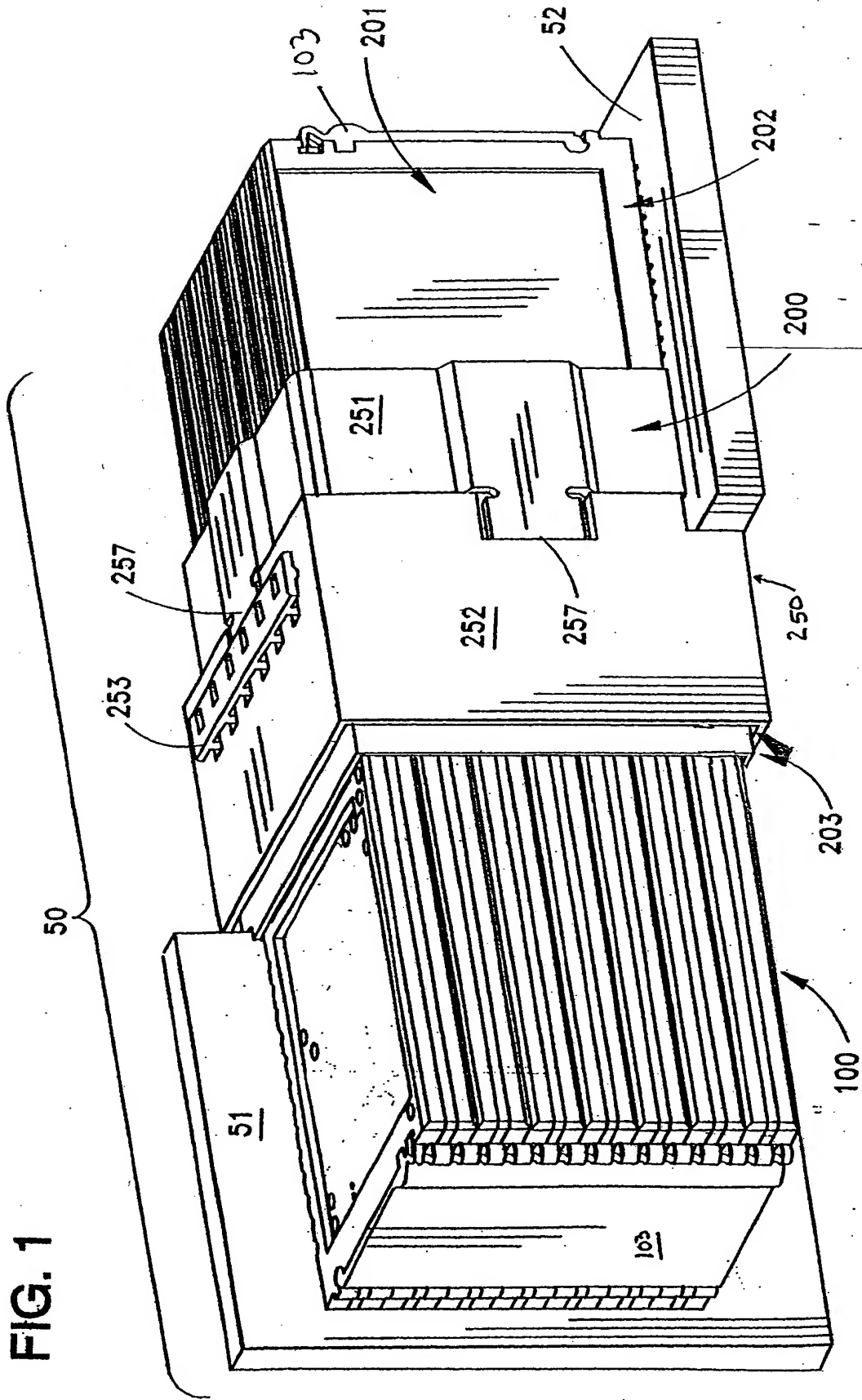
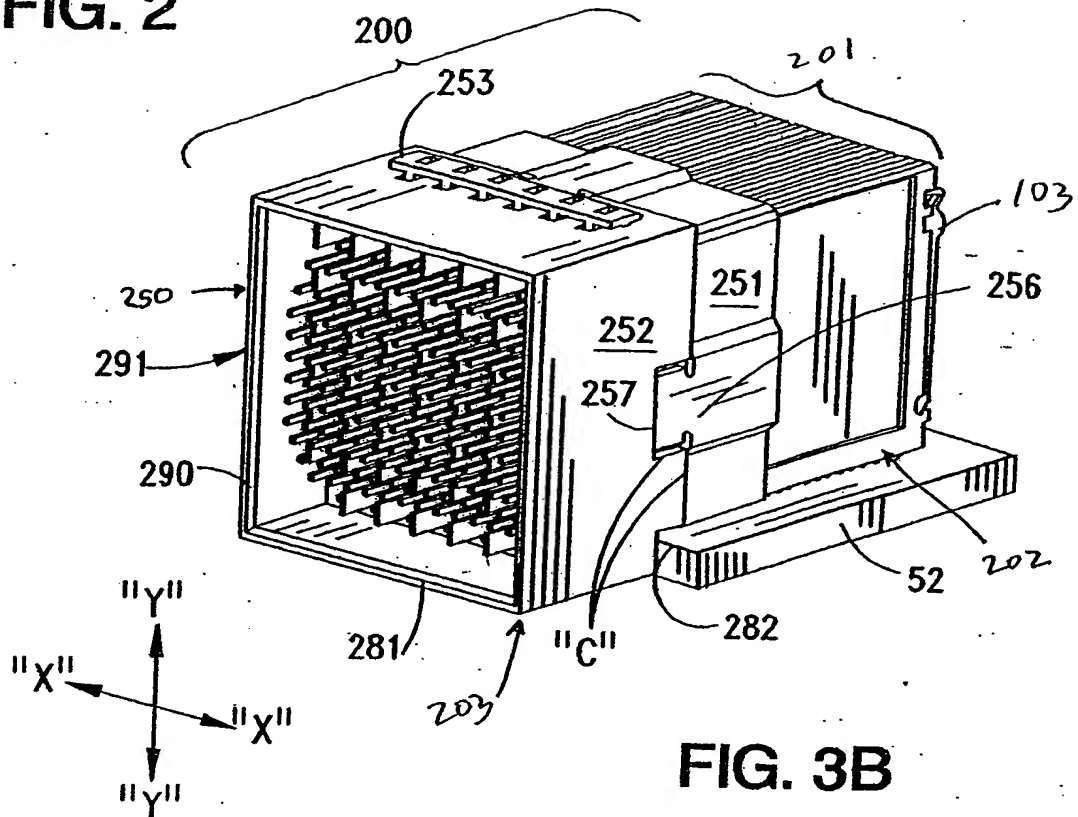


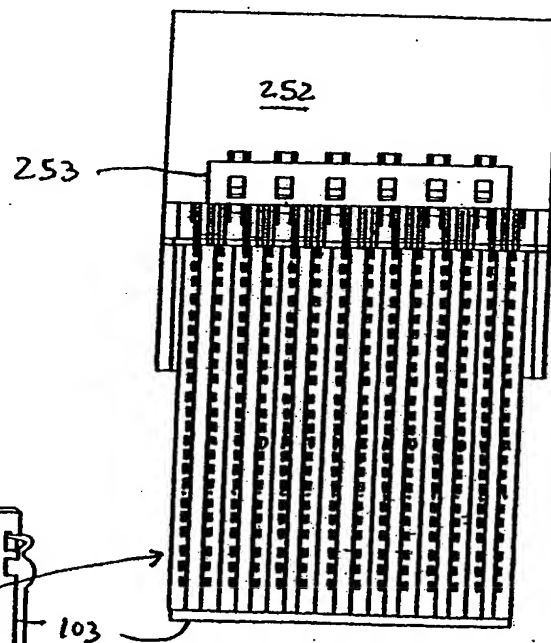
FIG. 1



**FIG. 2**



**FIG. 3B**



**FIG. 3A**

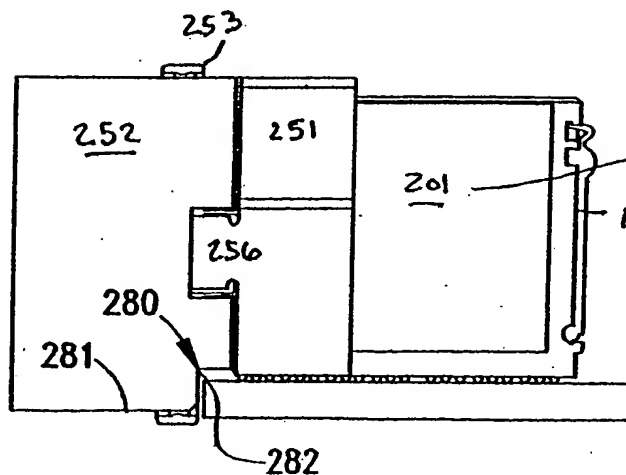


FIG. 4

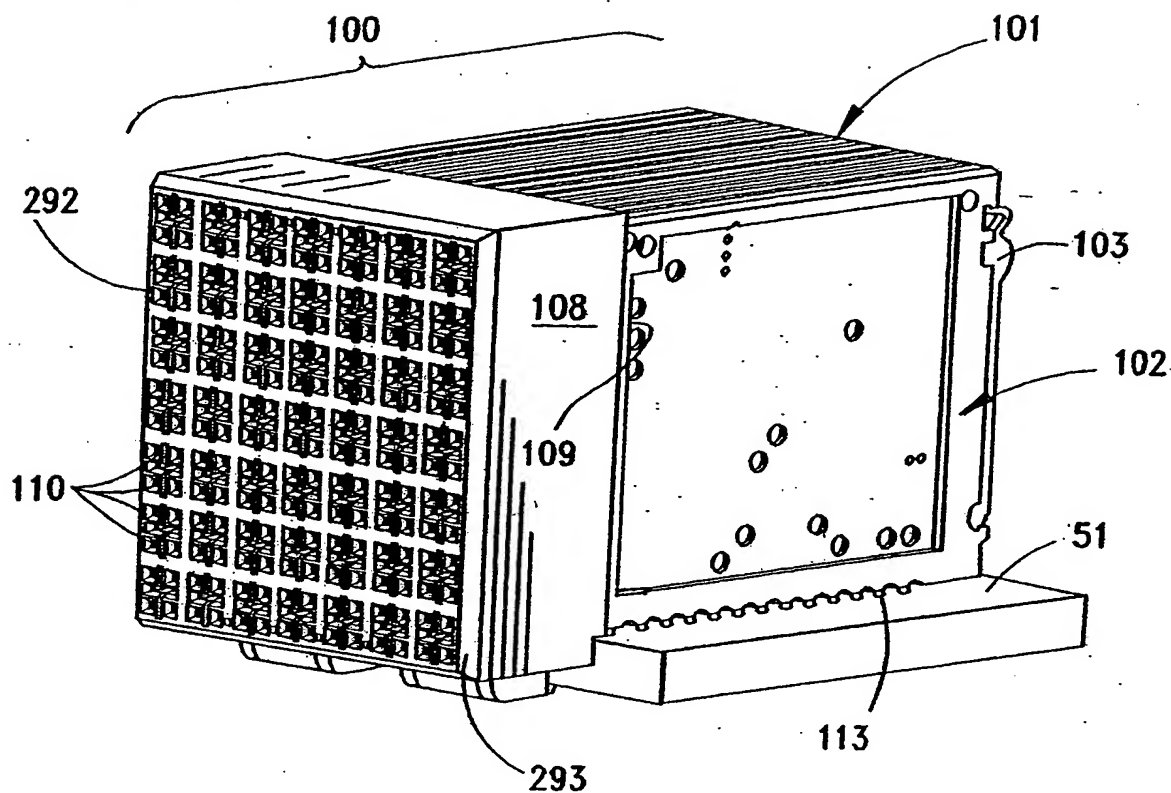


FIG. 5

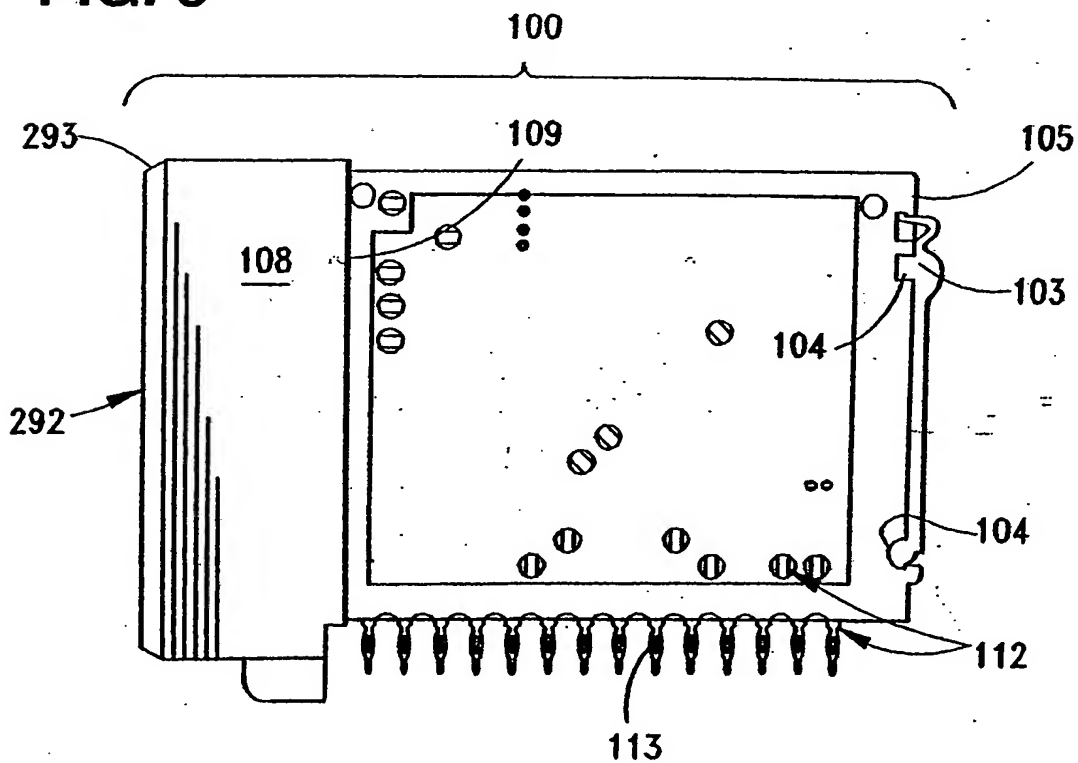
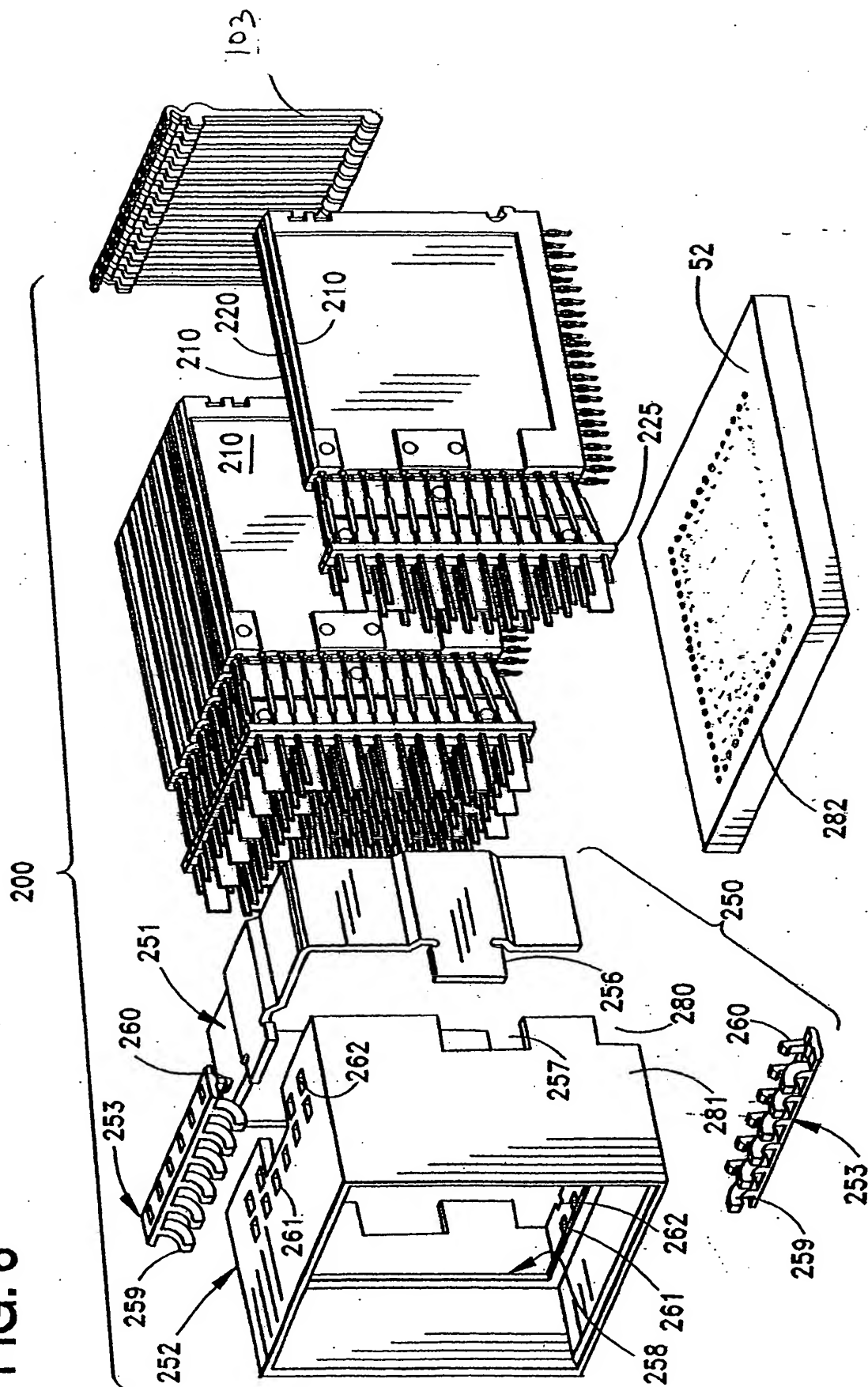
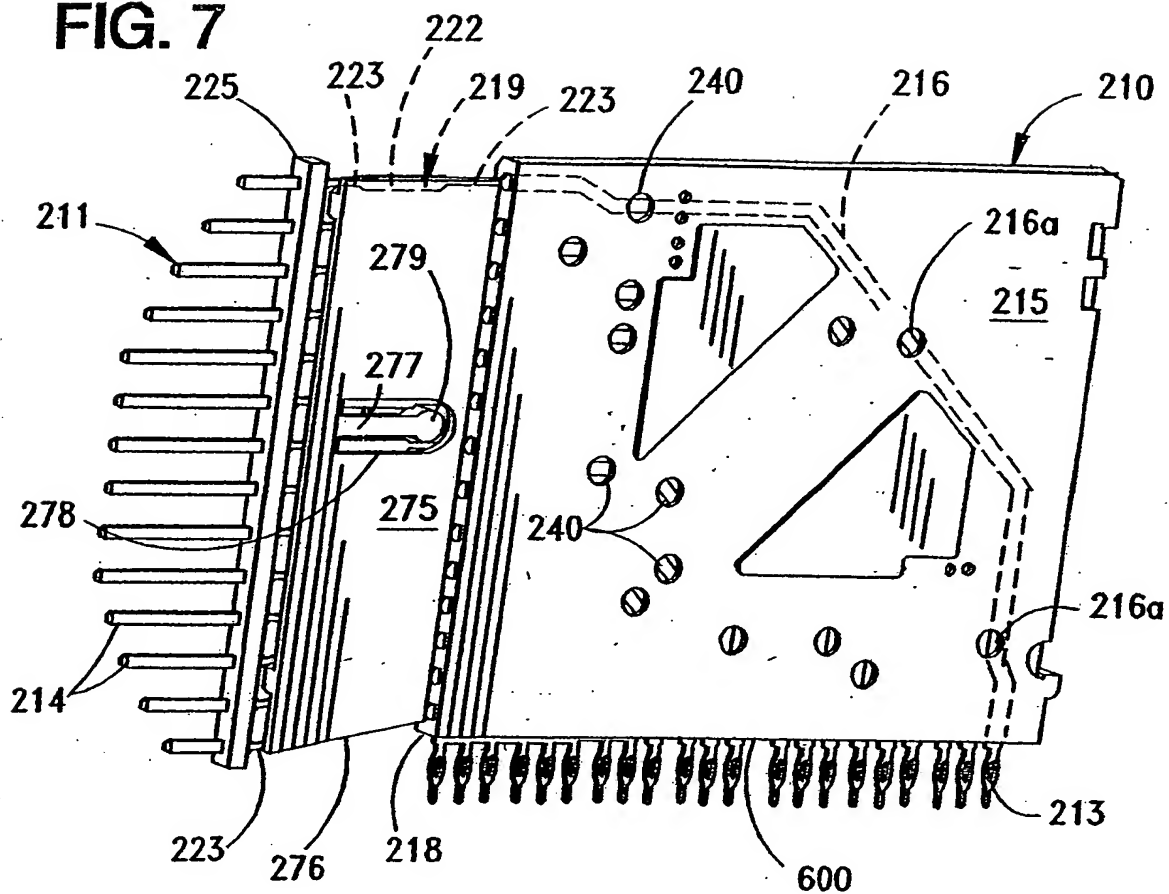


FIG. 6



**FIG. 7**



**FIG. 8**

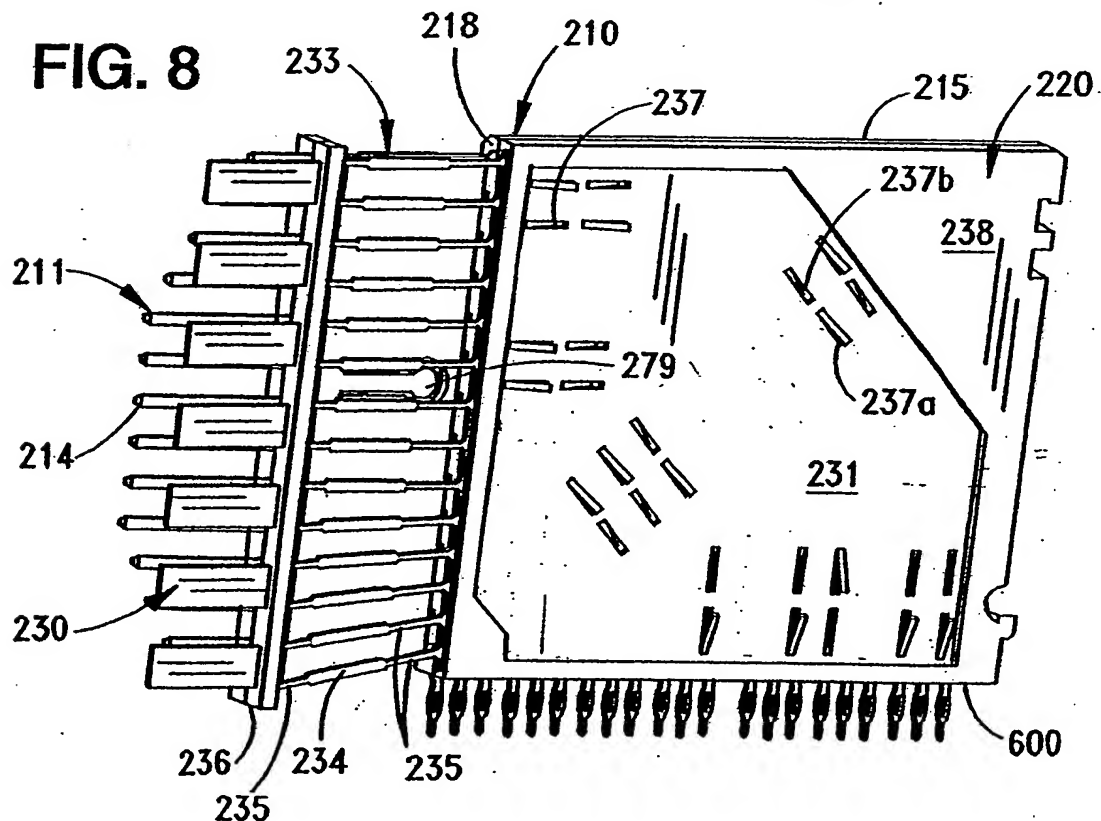
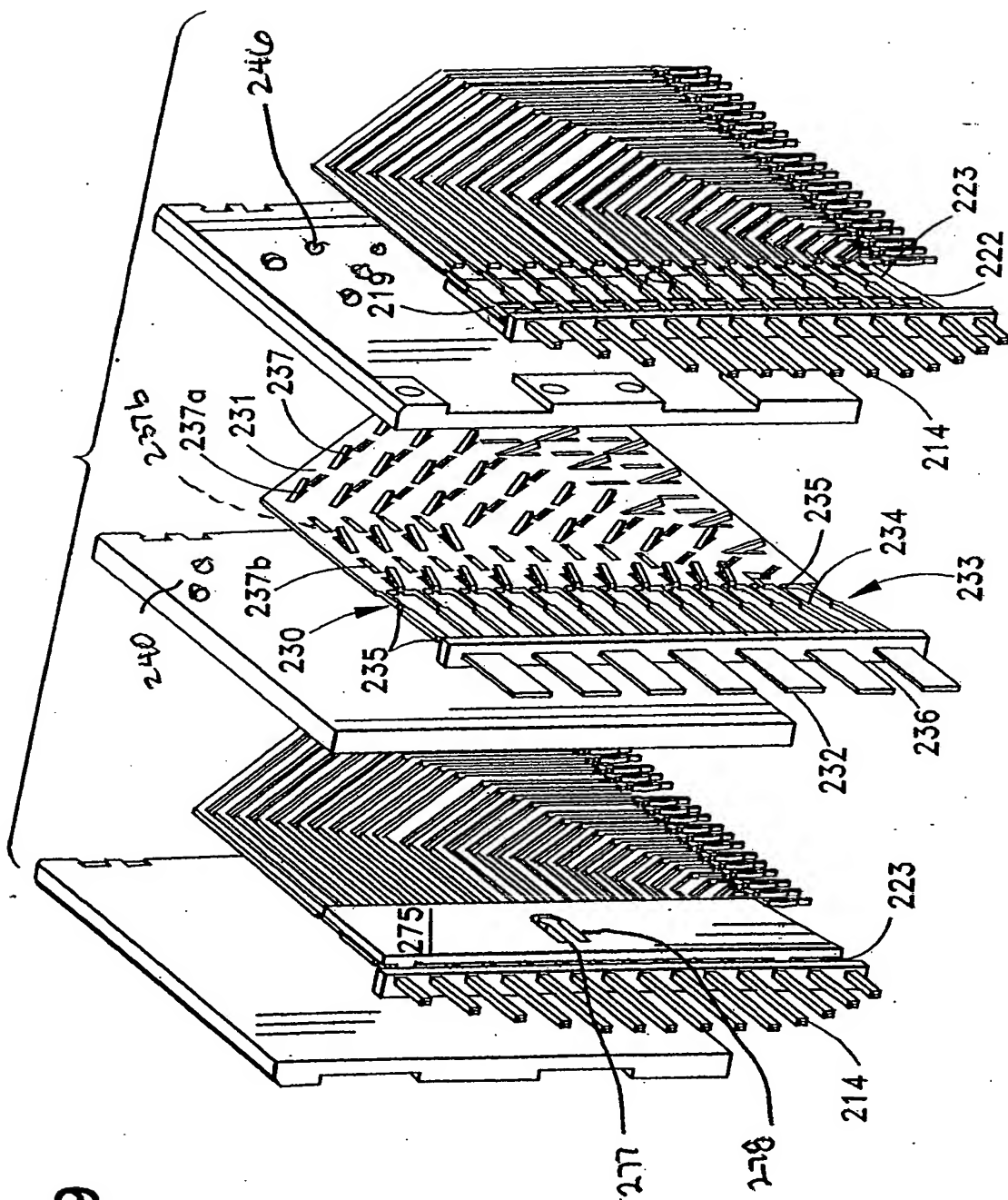


FIG. 9



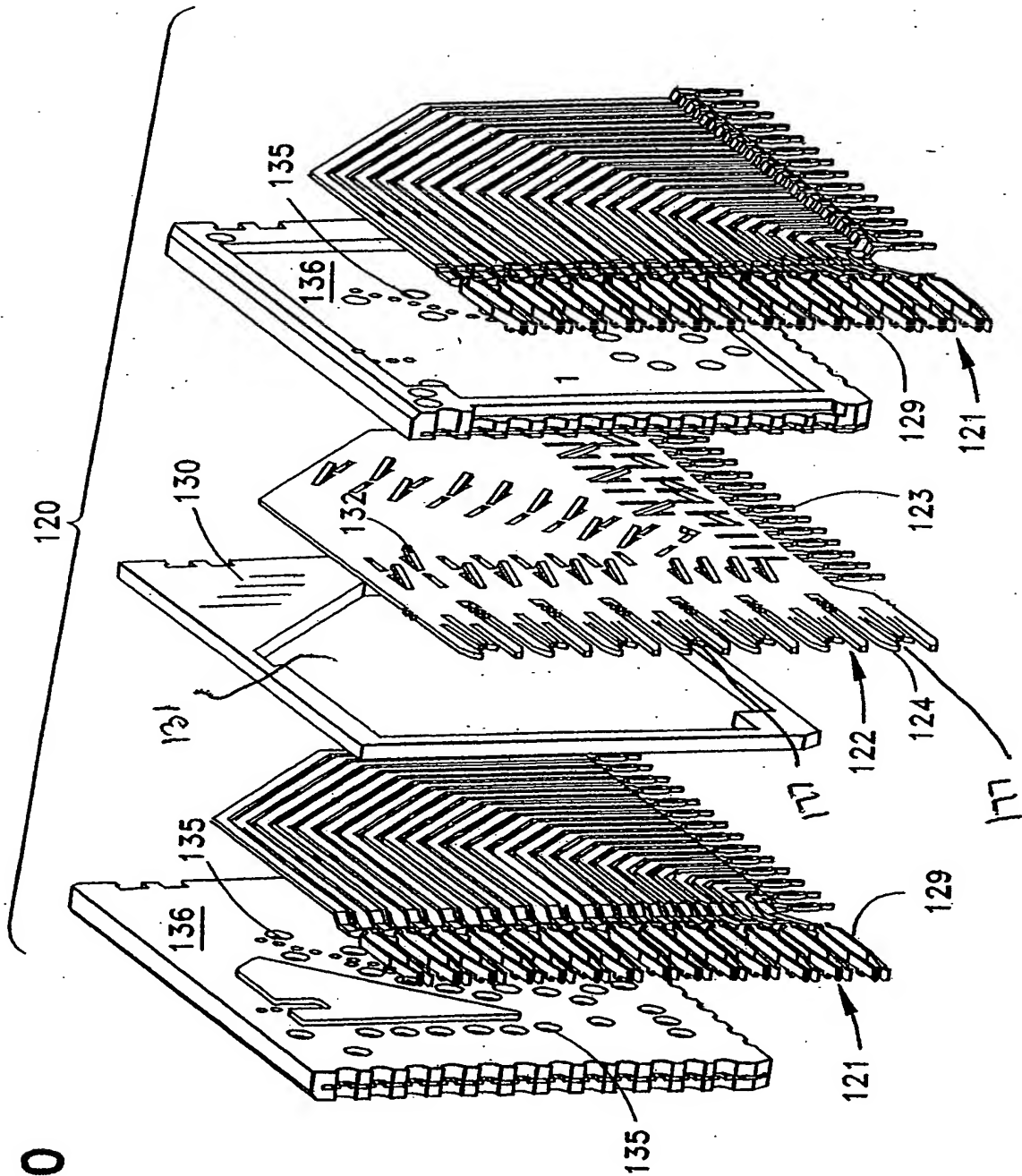
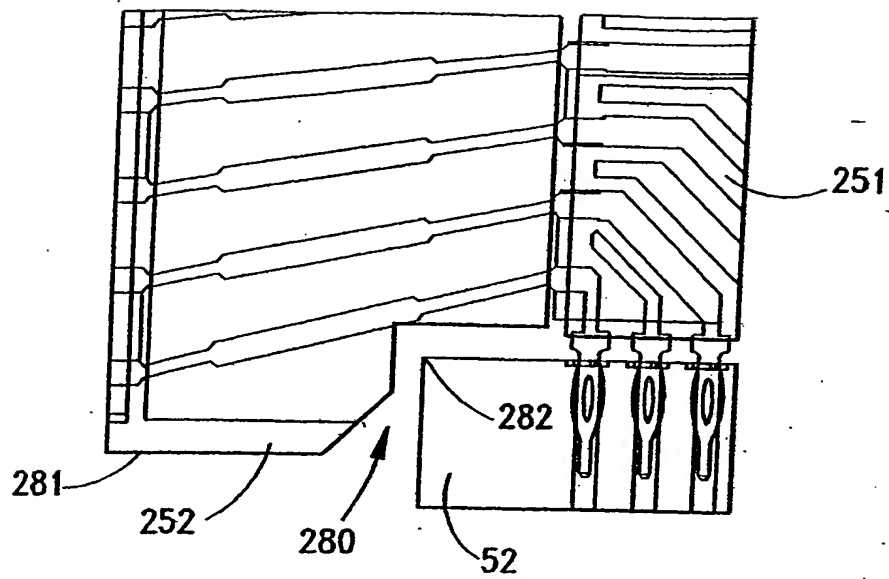


FIG. 1 is a perspective view of a fully flexed flexible circuit assembly 200. The assembly includes a substrate 201 with a conductive layer 251 and a conductive pad 252. A conductive trace 280 is shown on the conductive layer 251. The assembly is shown in a fully flexed state in the +Y direction.

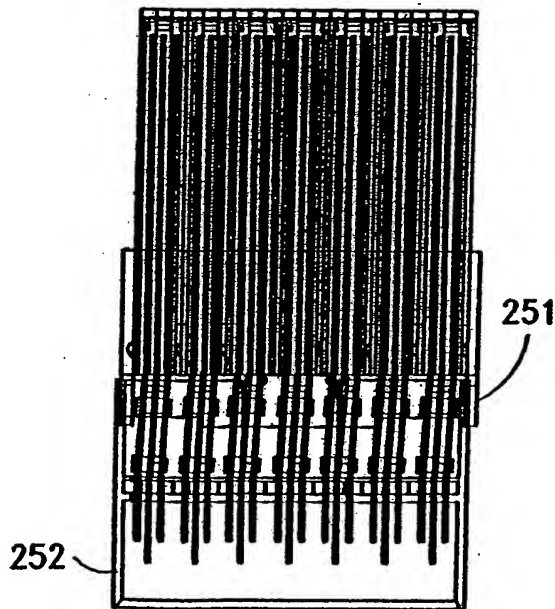
[illegible]



**FIG. 13**

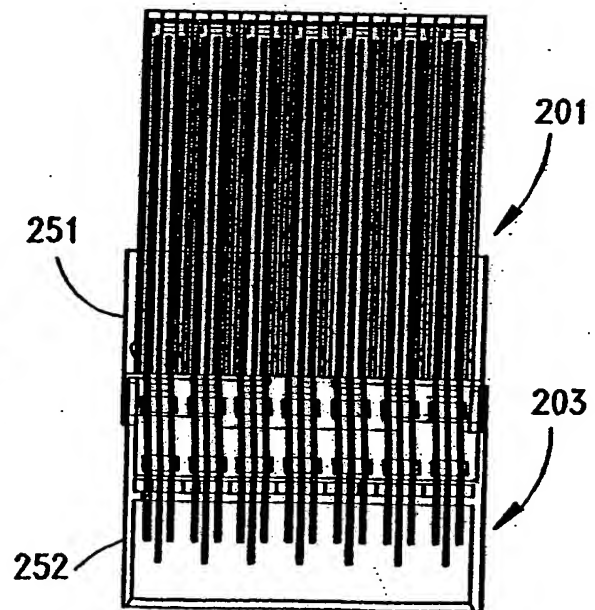


**FIG. 14**



FULLY FLEXED IN THE  
- DIRECTION

**FIG. 15**



FULLY FLEXED IN THE  
+ DIRECTION

FIG. 16

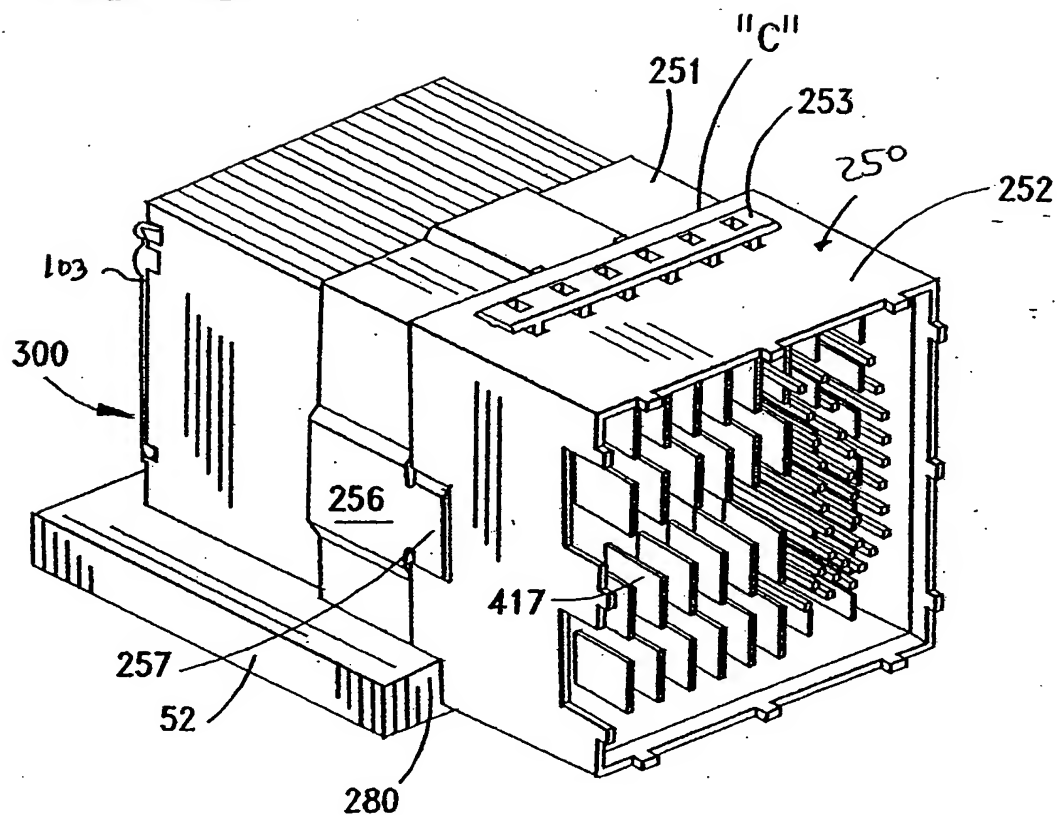


FIG. 17

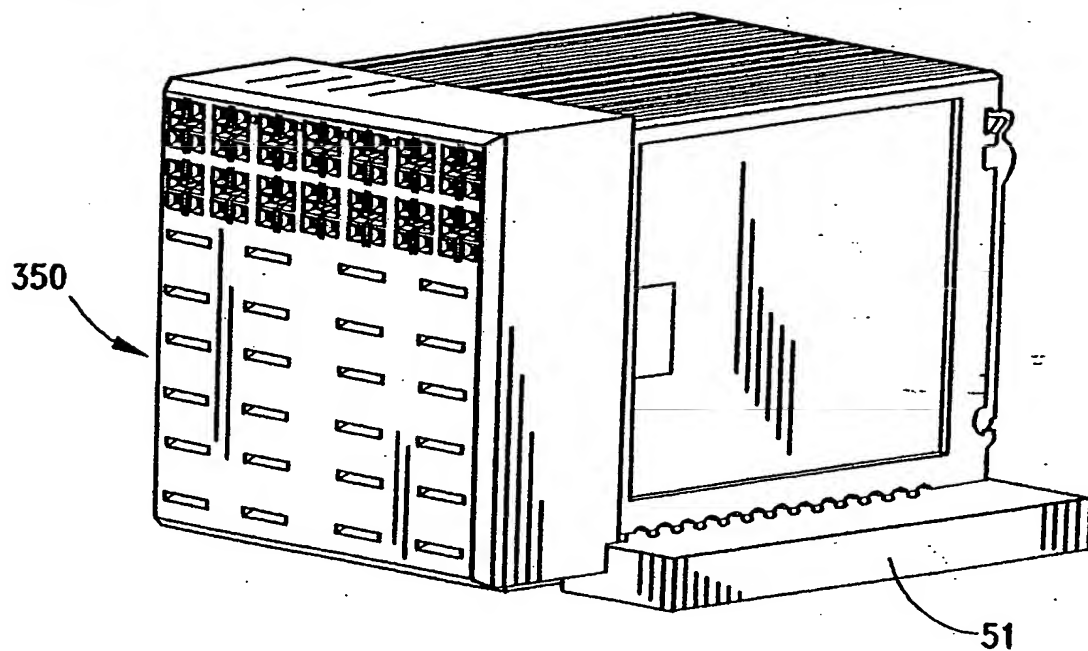


FIG. 18

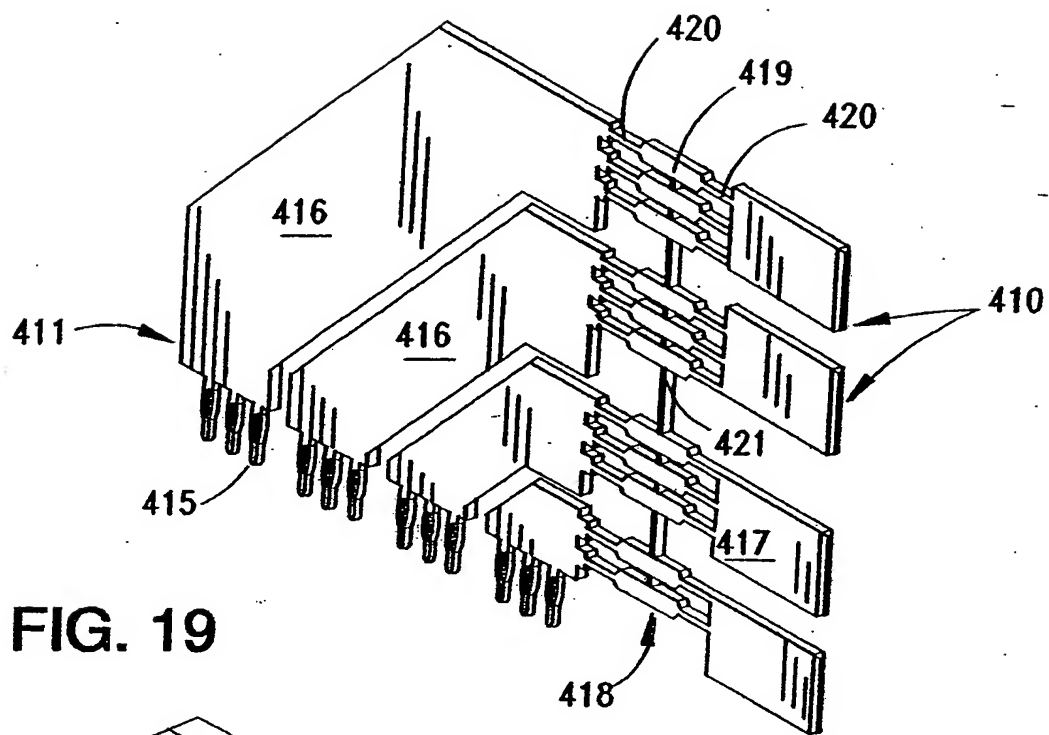


FIG. 19

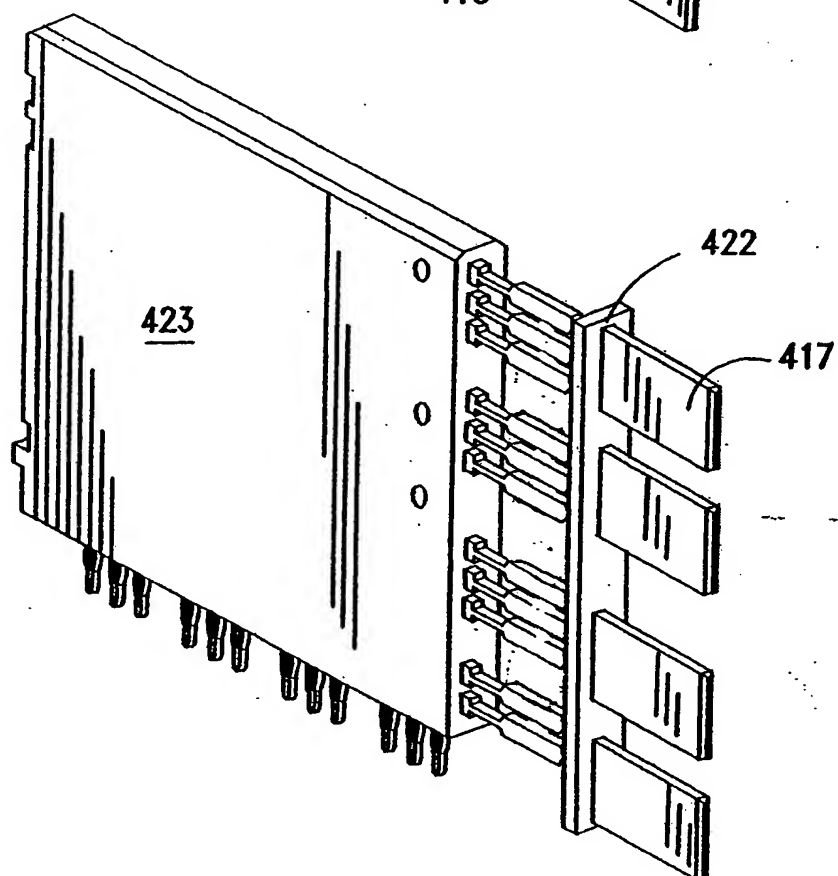


FIG. 20

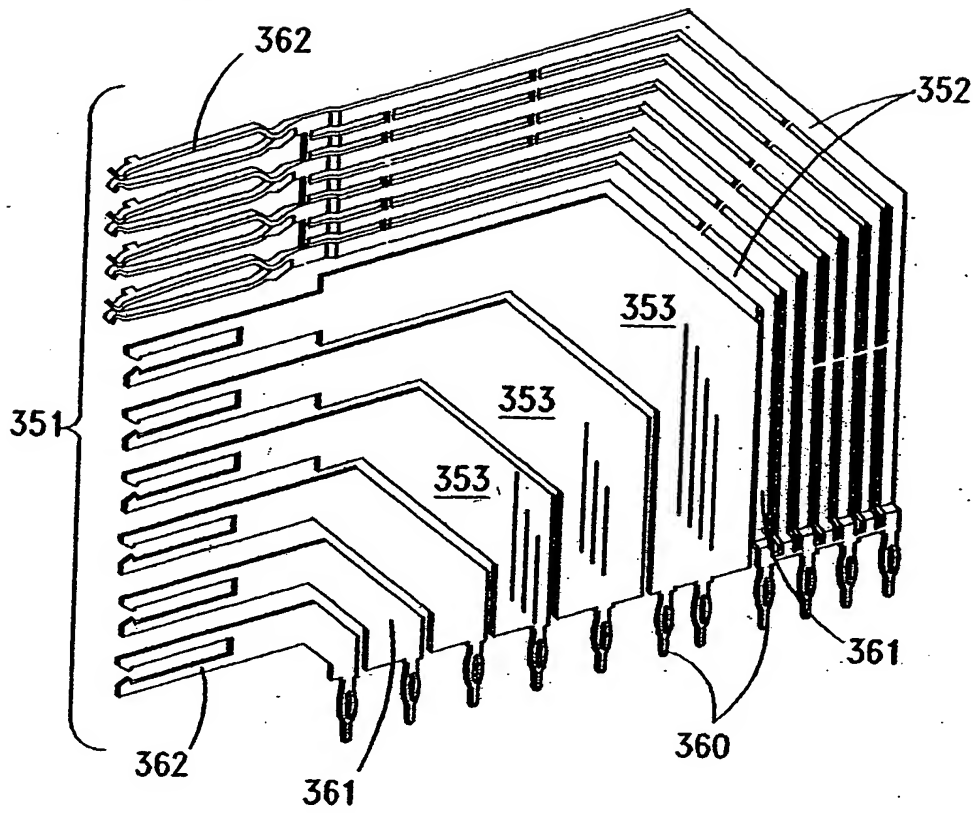


FIG. 21

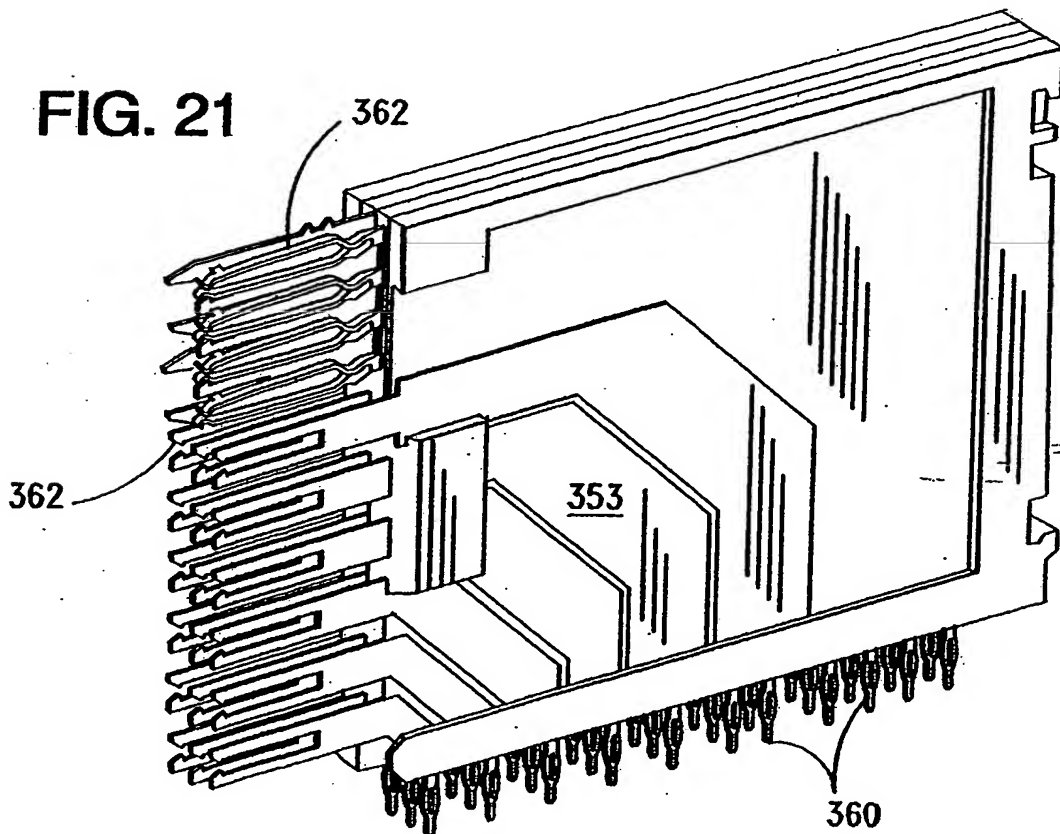


FIG. 22

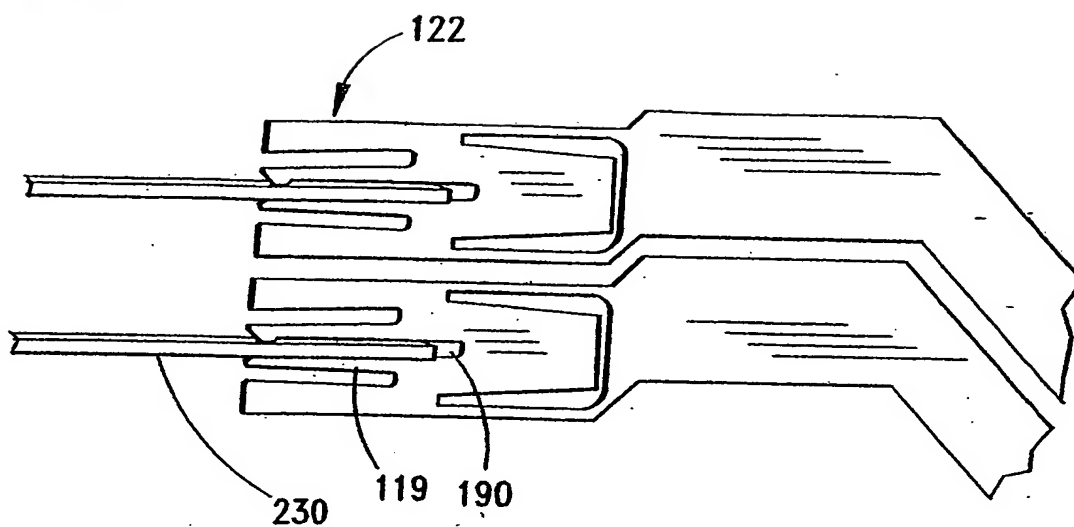


FIG. 23

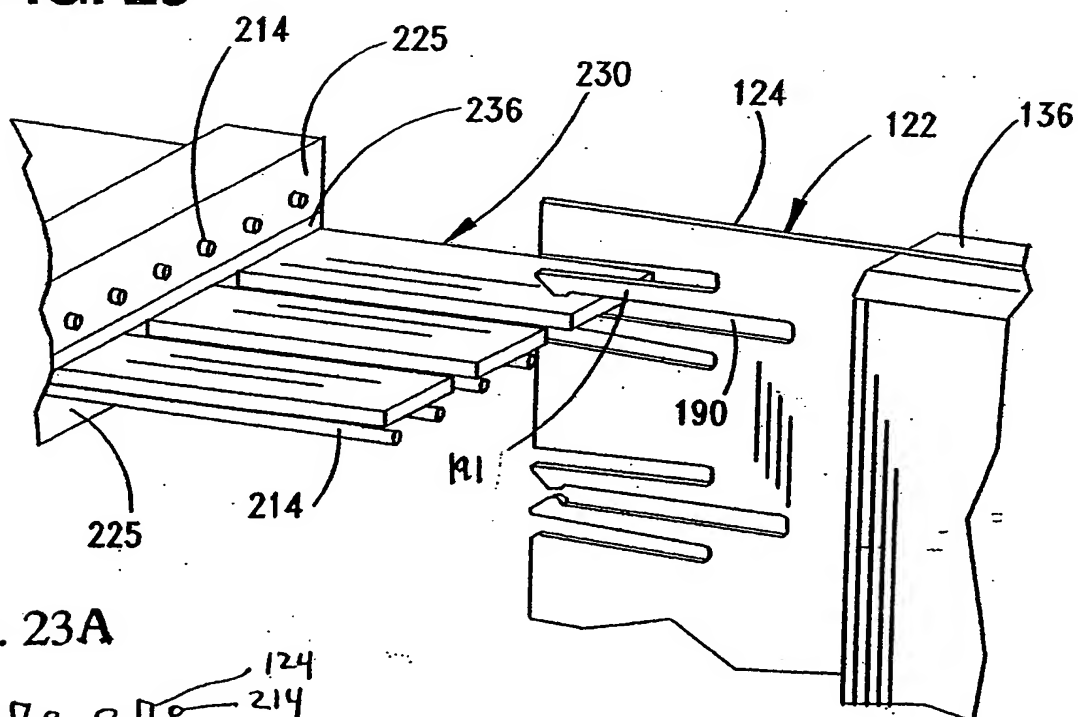


FIG. 23A

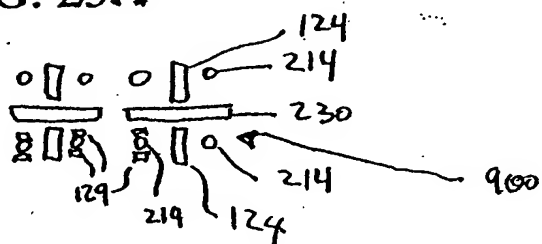




FIG. 24A

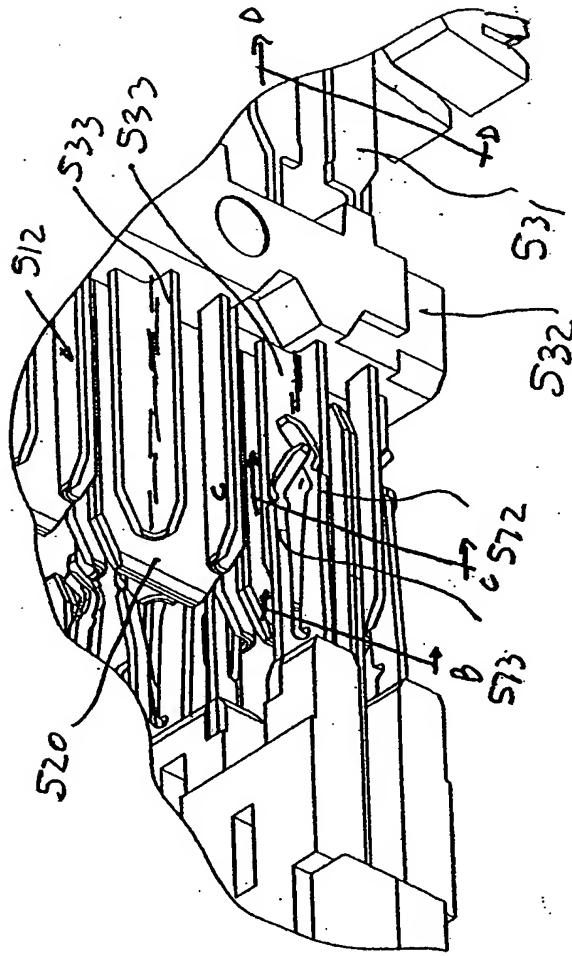


FIG. 24B

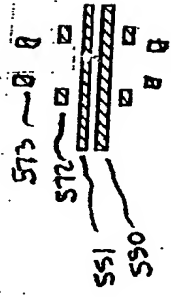


FIG. 24C

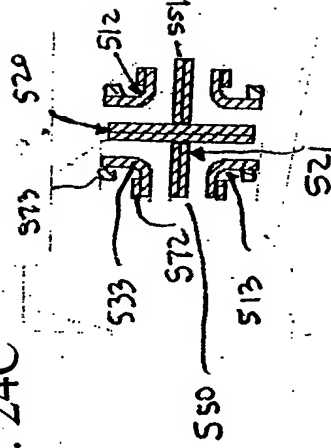


FIG. 24D

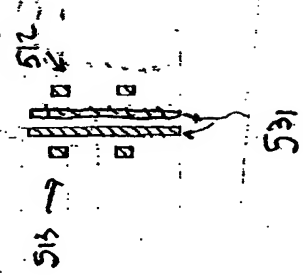


FIG. 25

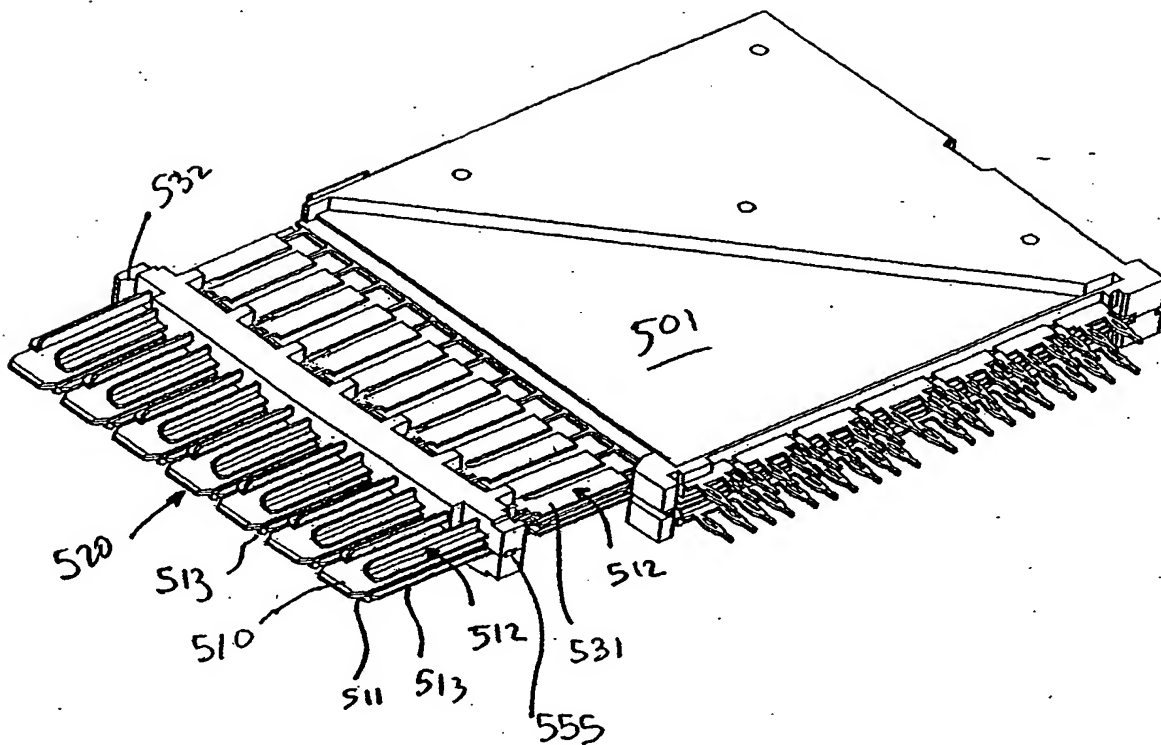


FIG. 26

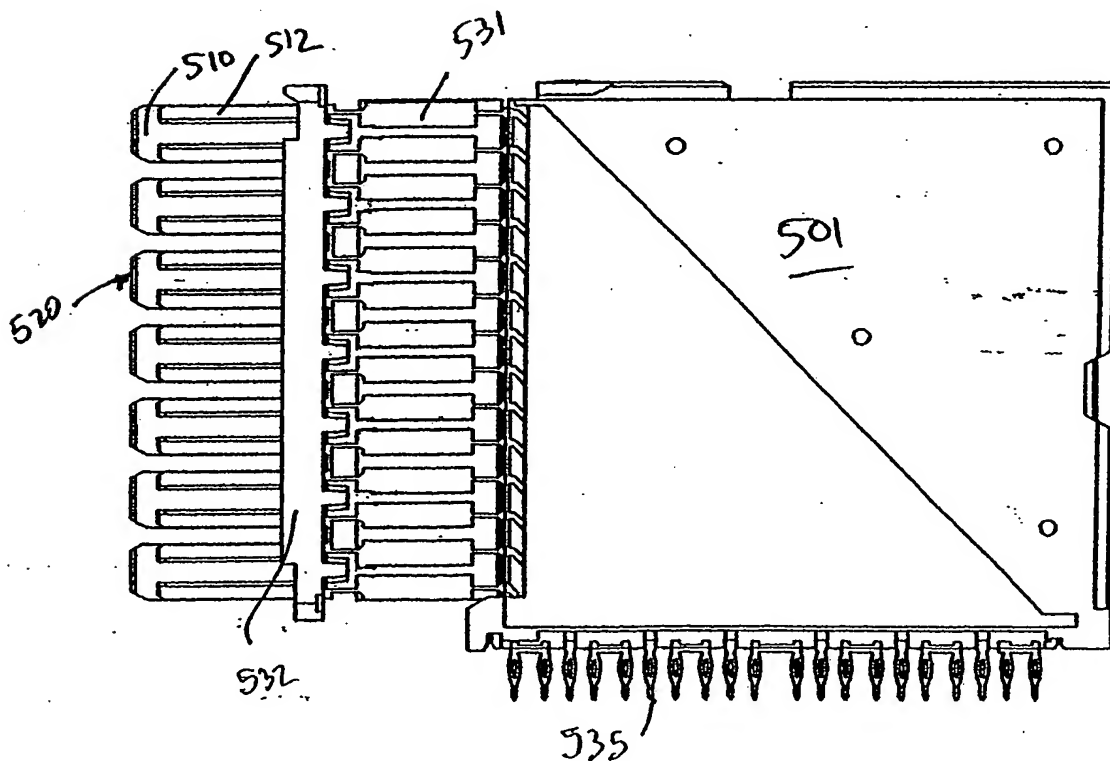




FIG. 27

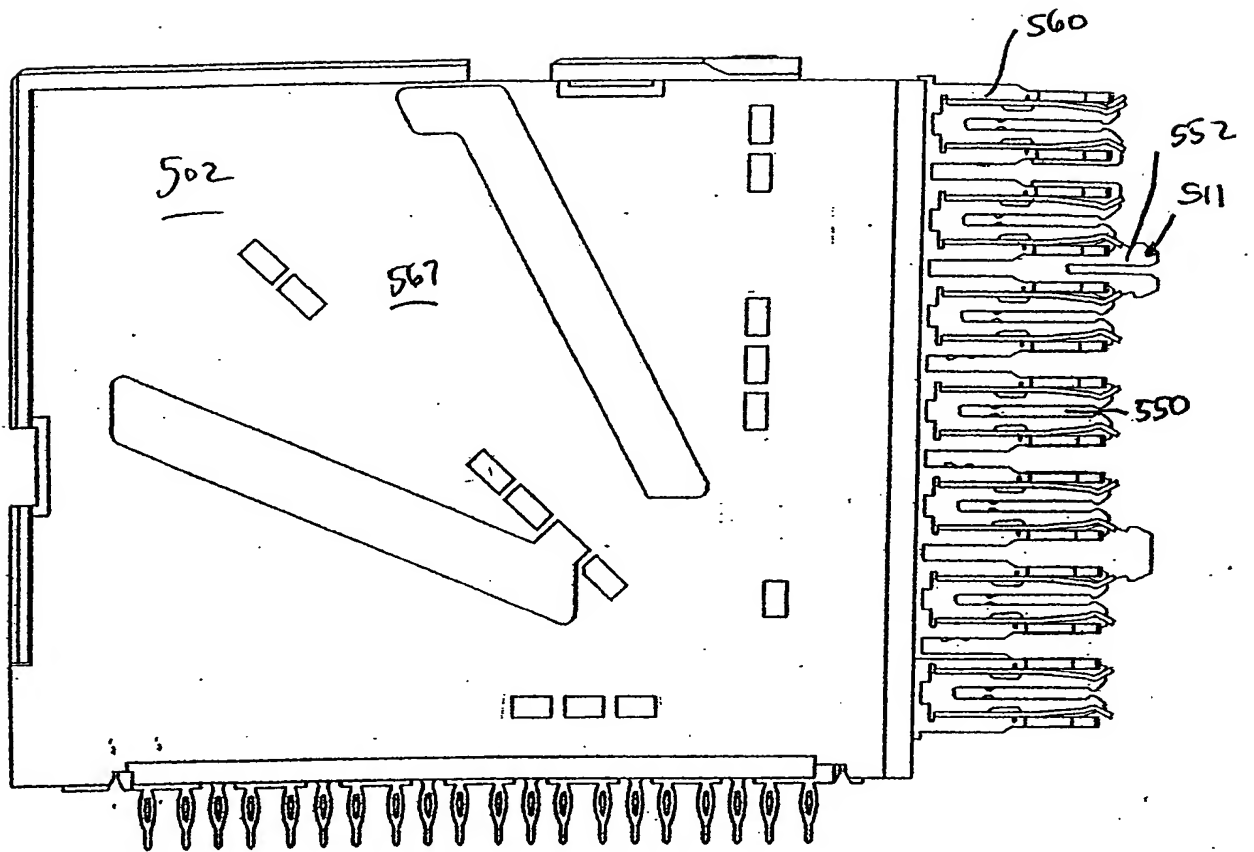


FIG. 28

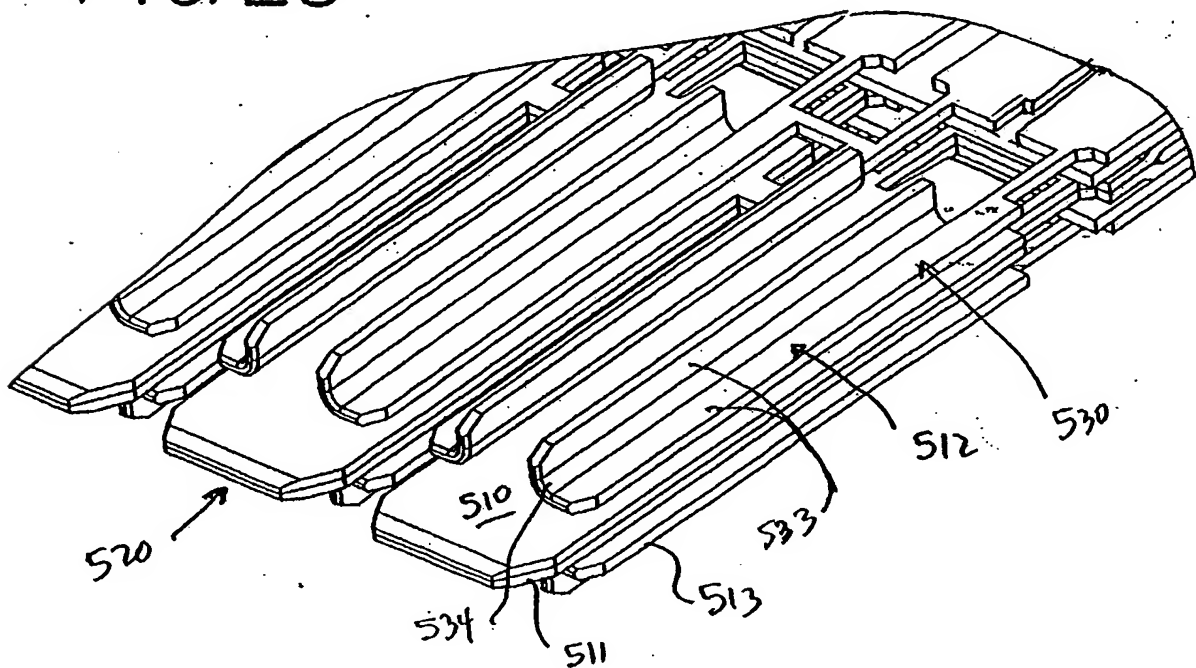


FIG. 29

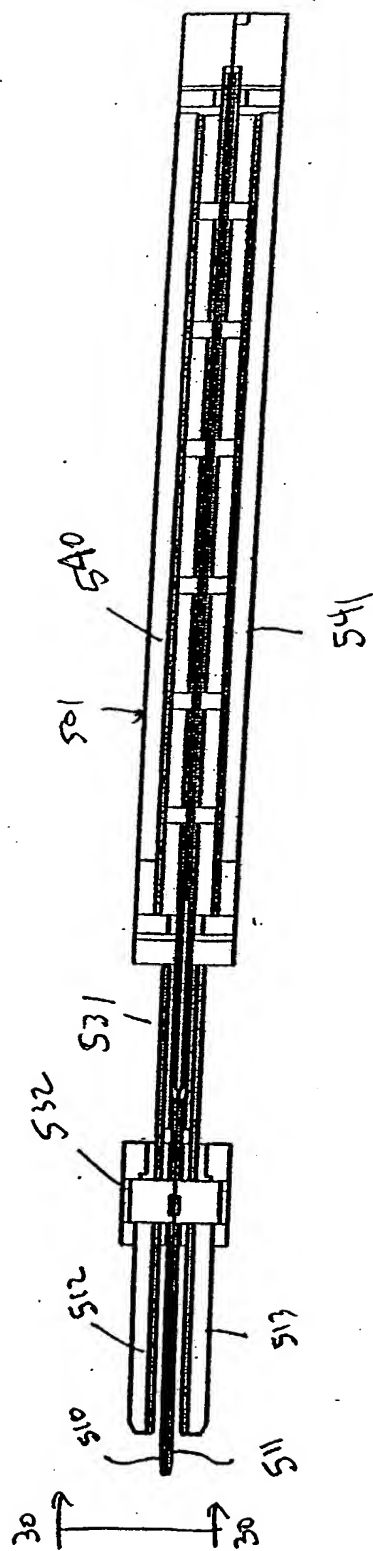


FIG. 30

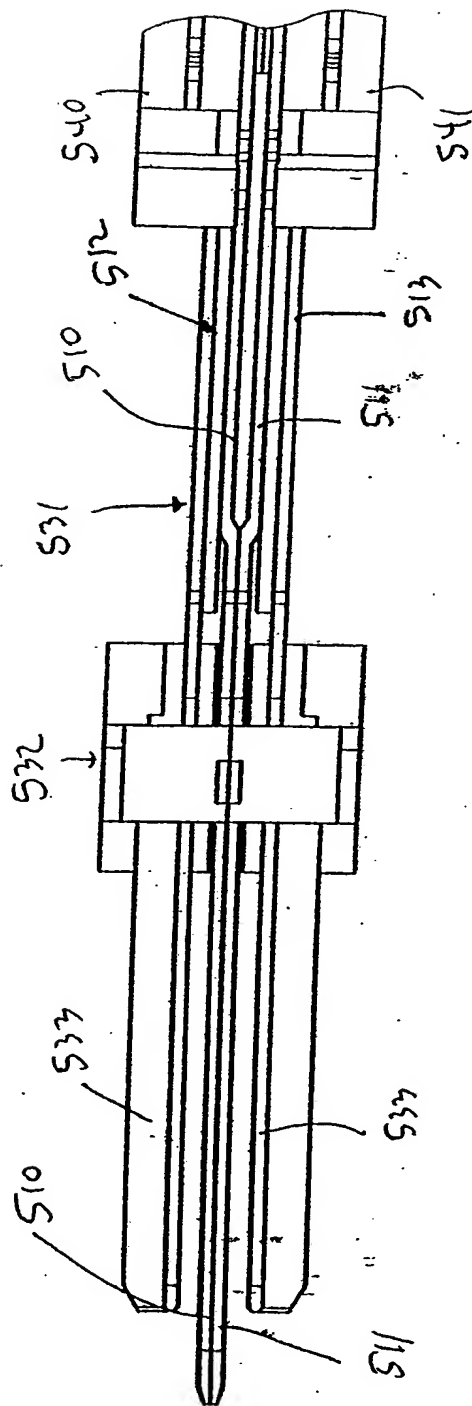


FIG. 31

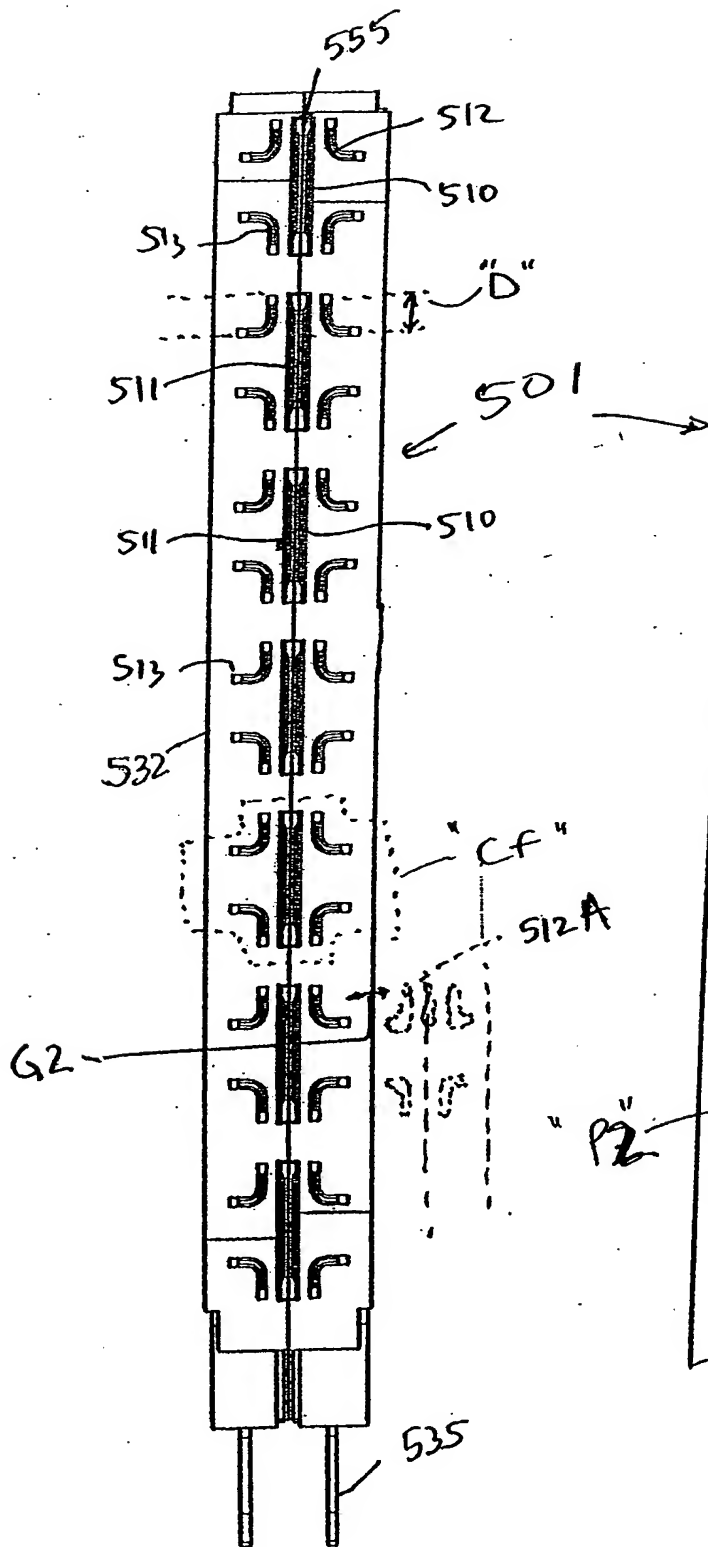


FIG. 32

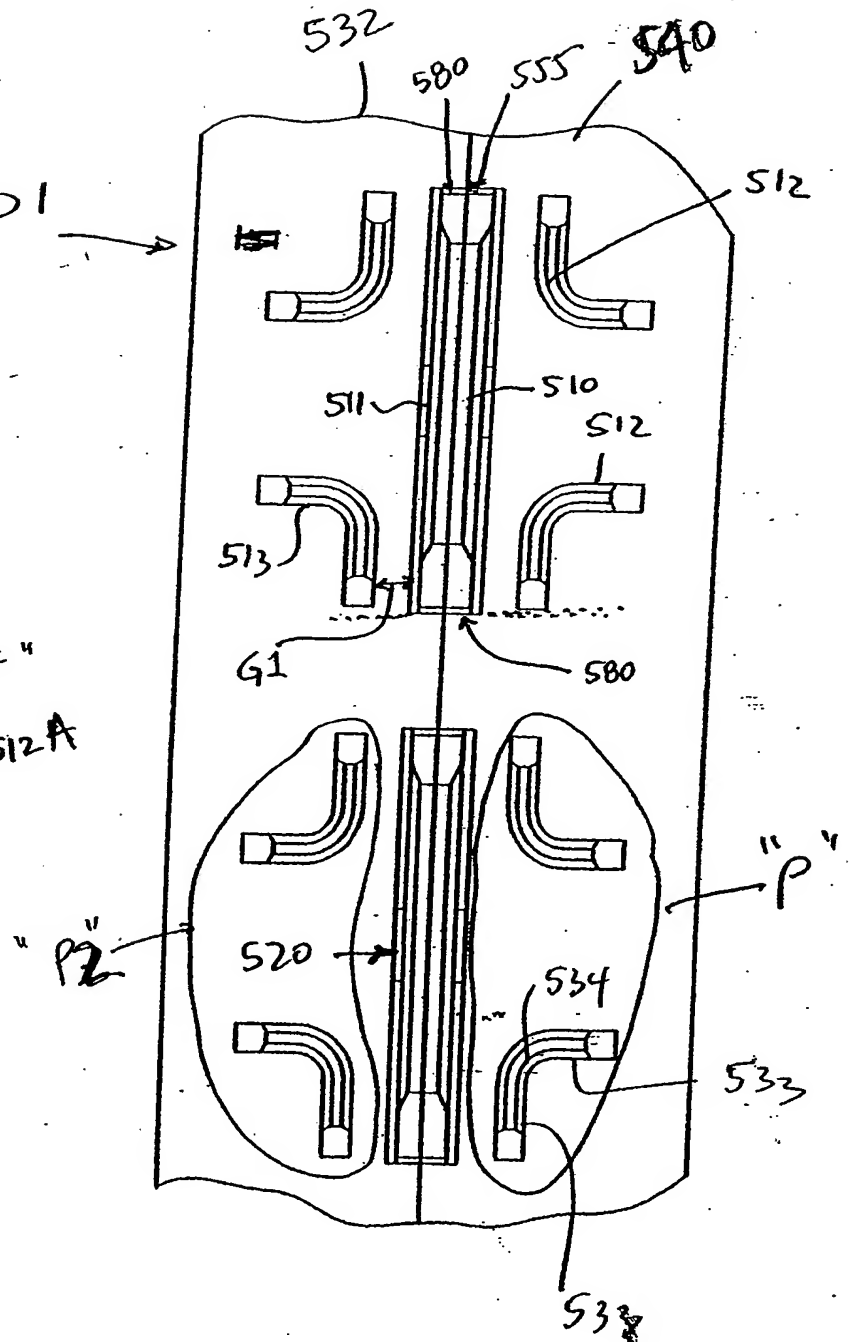


FIG. 33 is a perspective view of a multi-layered electronic assembly. The assembly consists of several stacked layers. A circular inset provides a magnified view of a specific region on the right side of the assembly. In this magnified view, a central rectangular block (541) is shown, surrounded by various conductive traces and pads. Labels 545 and 546 point to specific features on the central block. Labels 535 and 540 point to surrounding structures. Labels 510 and 511 point to other components. The main assembly is labeled with 501, 531, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600.

FIG. 34

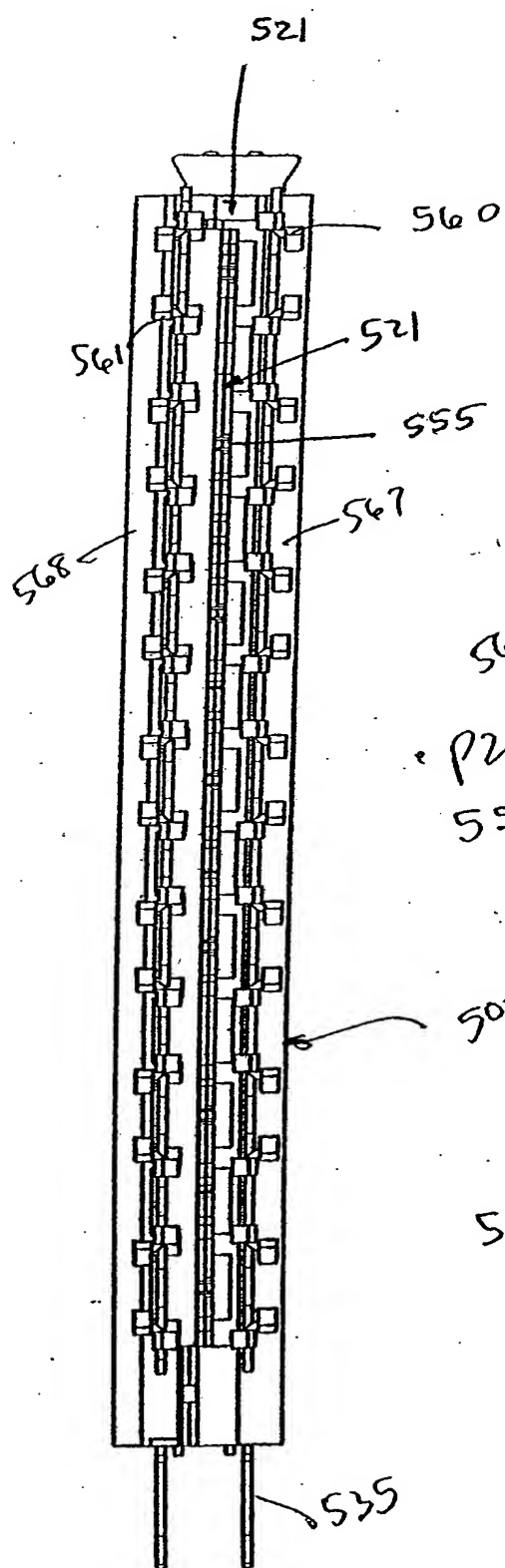


FIG. 35

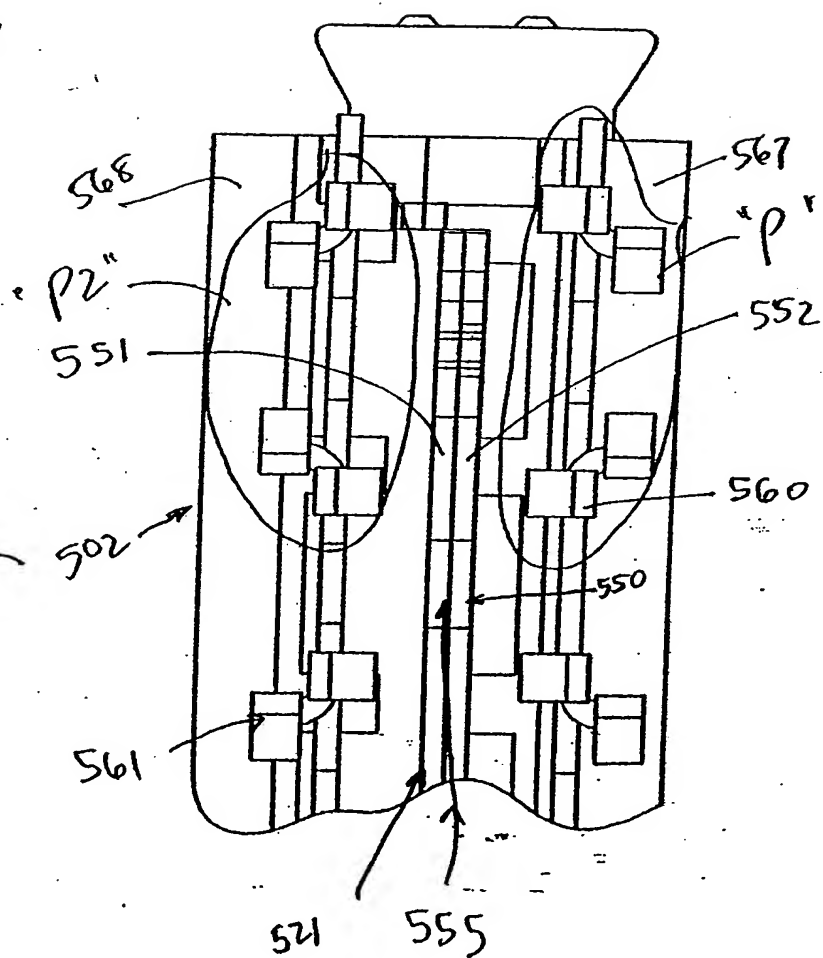


FIG. 36

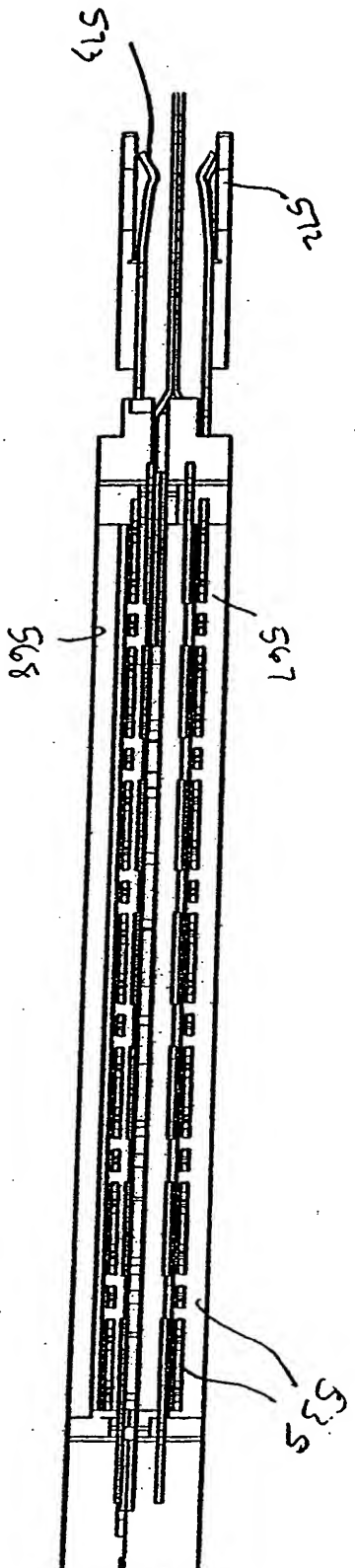


FIG. 37

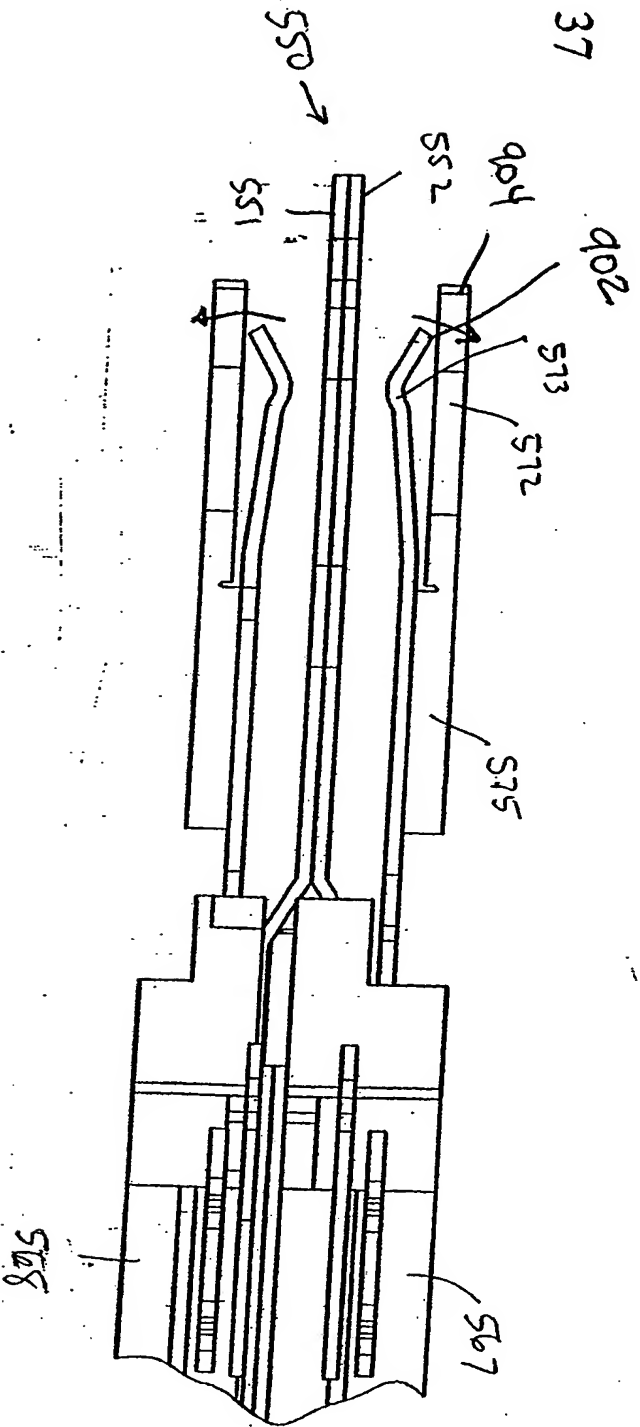


FIG. 38

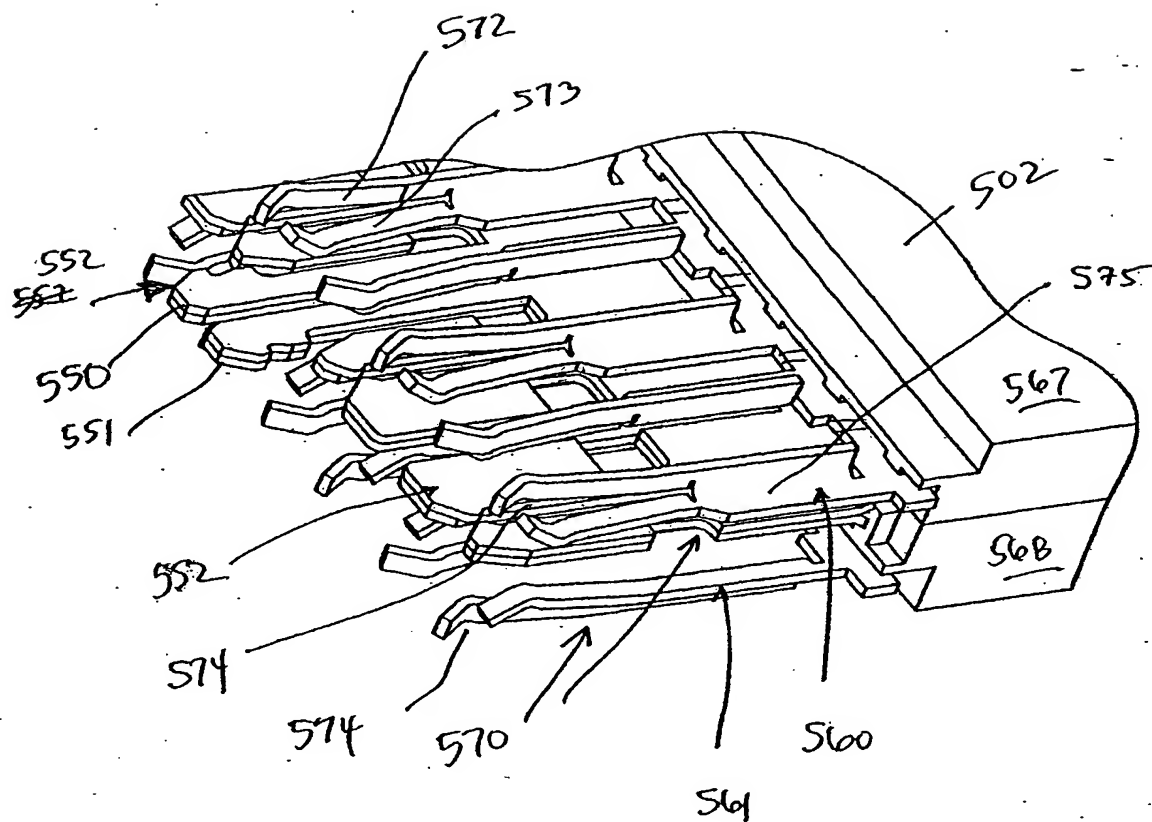


FIG. 39

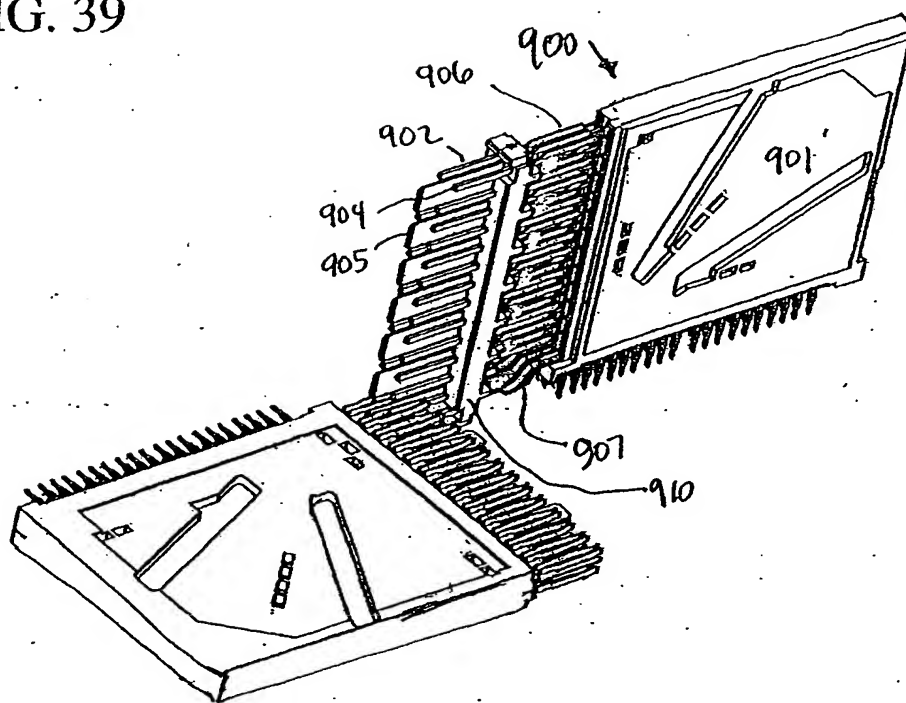




FIG. 40

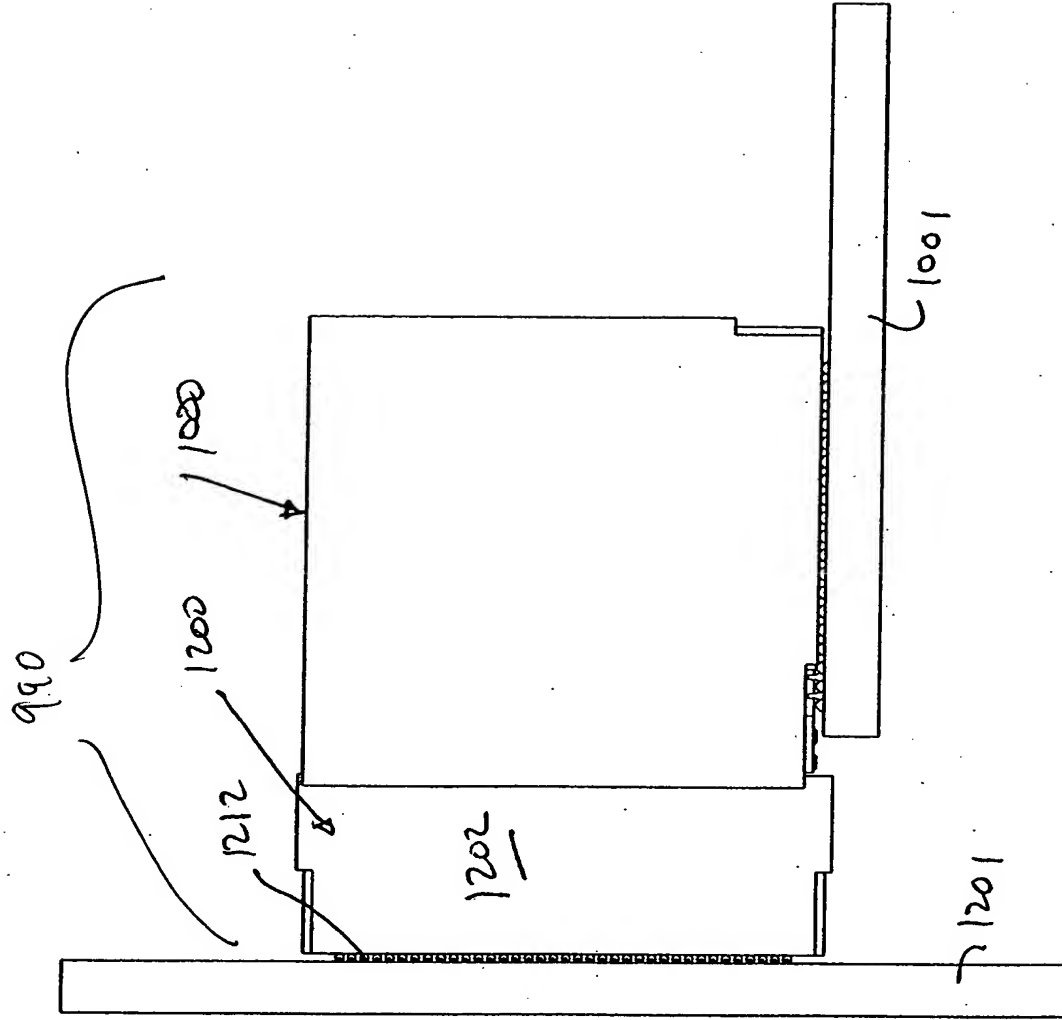


FIG. 41

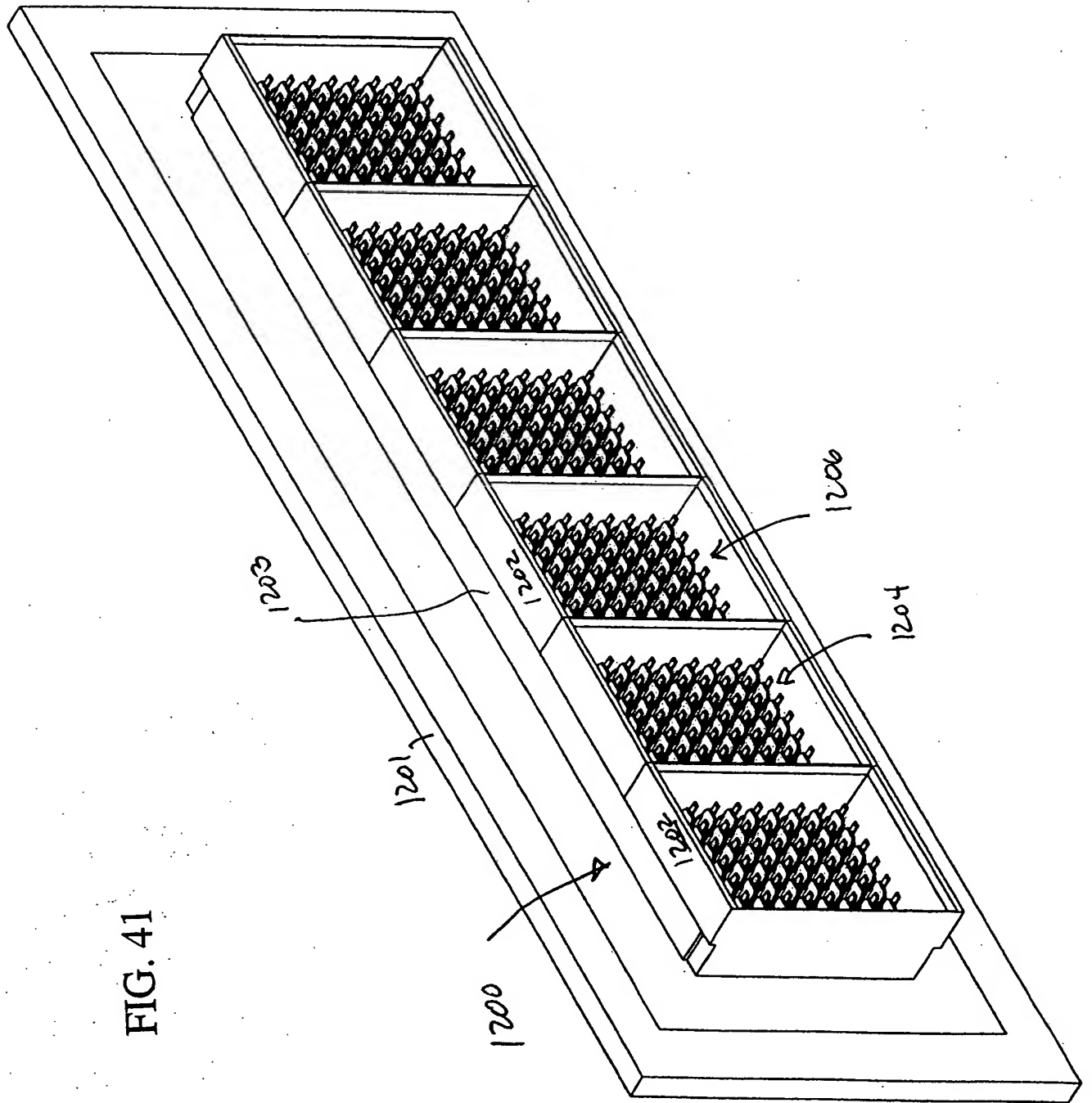


FIG. 42

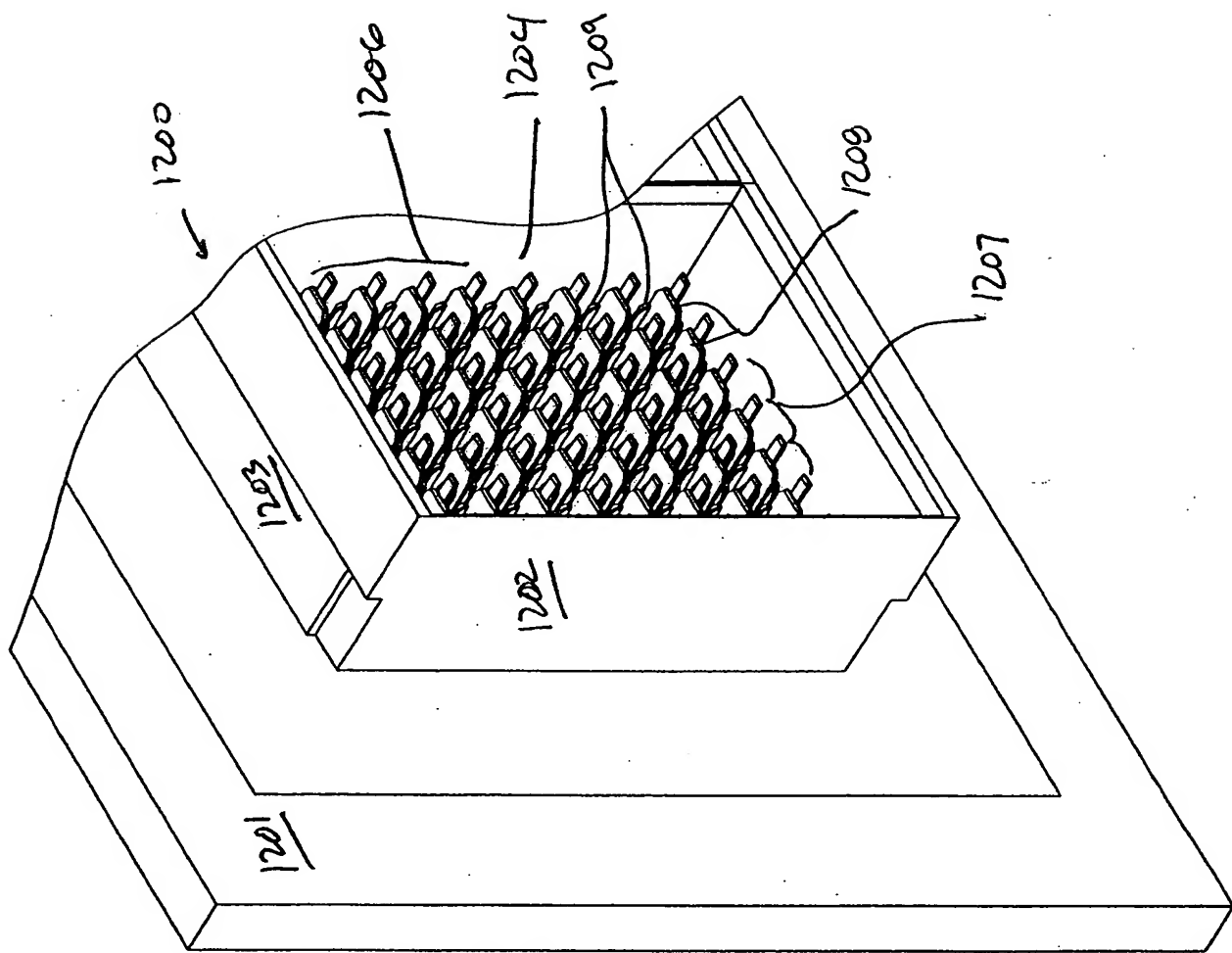


FIG. 43

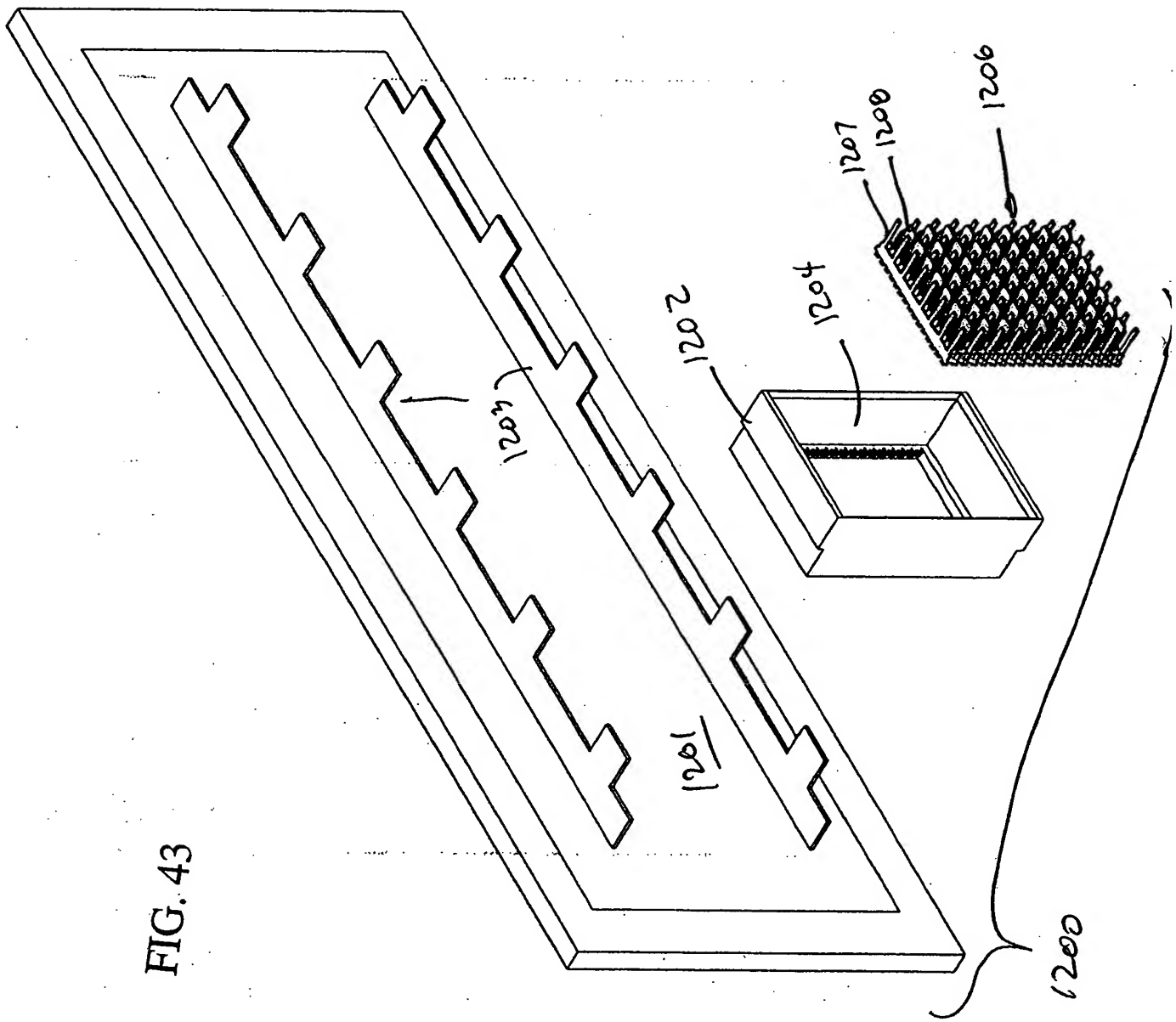
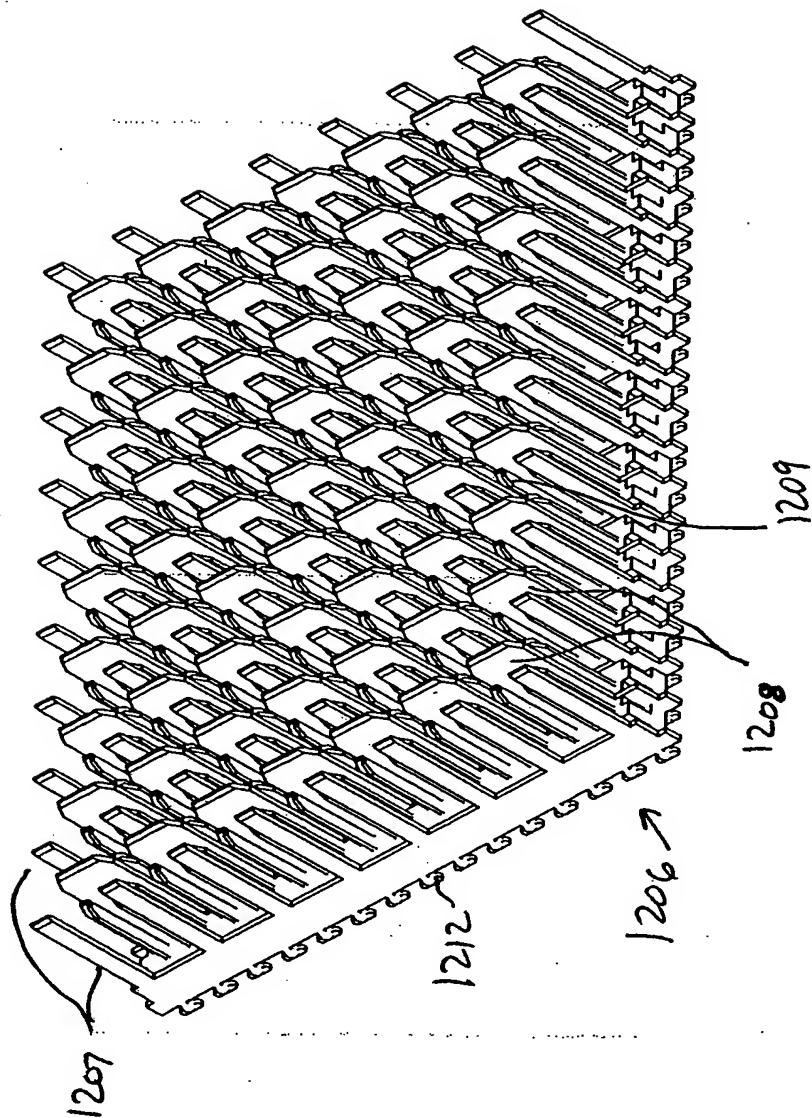


FIG. 44



11

FIG. 46

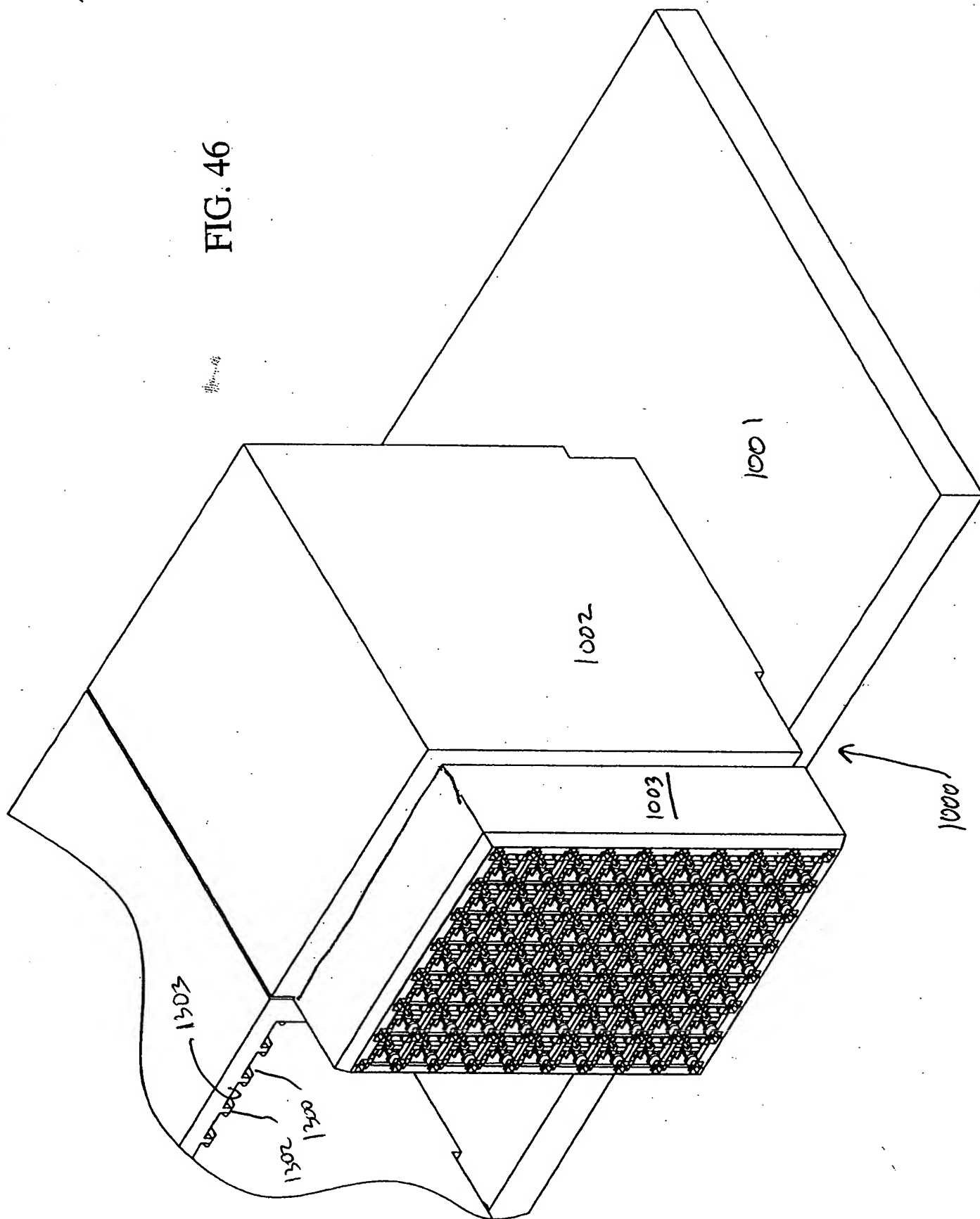
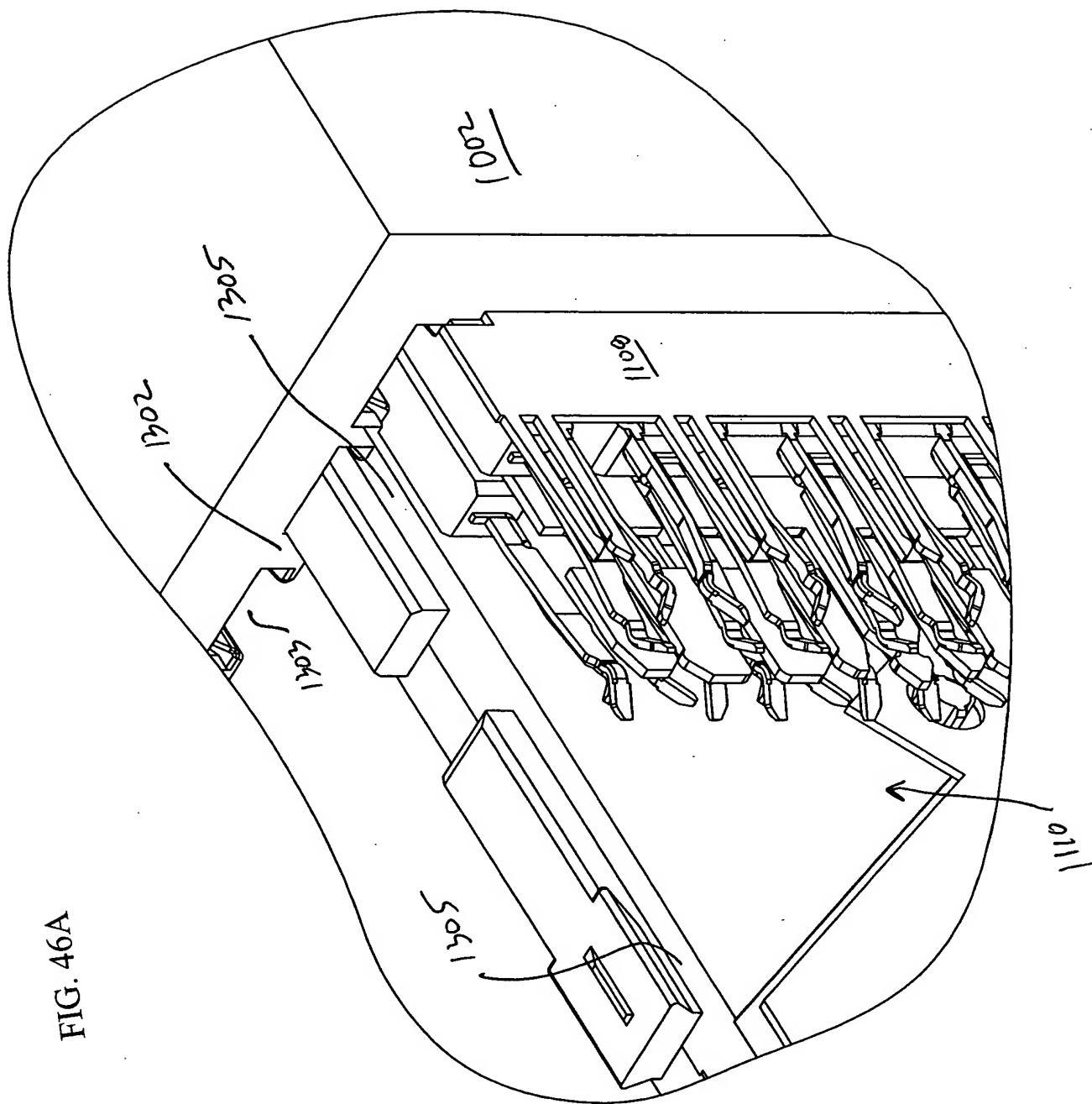


FIG. 46A





**FIG. 47**

The diagram illustrates a multi-layered electronic device assembly in three cross-sectional views. The top view shows a substrate 1106 with a layer 1121, a central stack of layers 1101-1104, and a side layer 1108. The middle view shows a similar assembly with labels 1101, 1102, 1103, 1104, 1105, 1109, 1120, and 1130. The bottom view shows a substrate 1106 with a layer 1121, a central stack of layers 1101-1104, and a side layer 1108. Arrows indicate connections between the components.

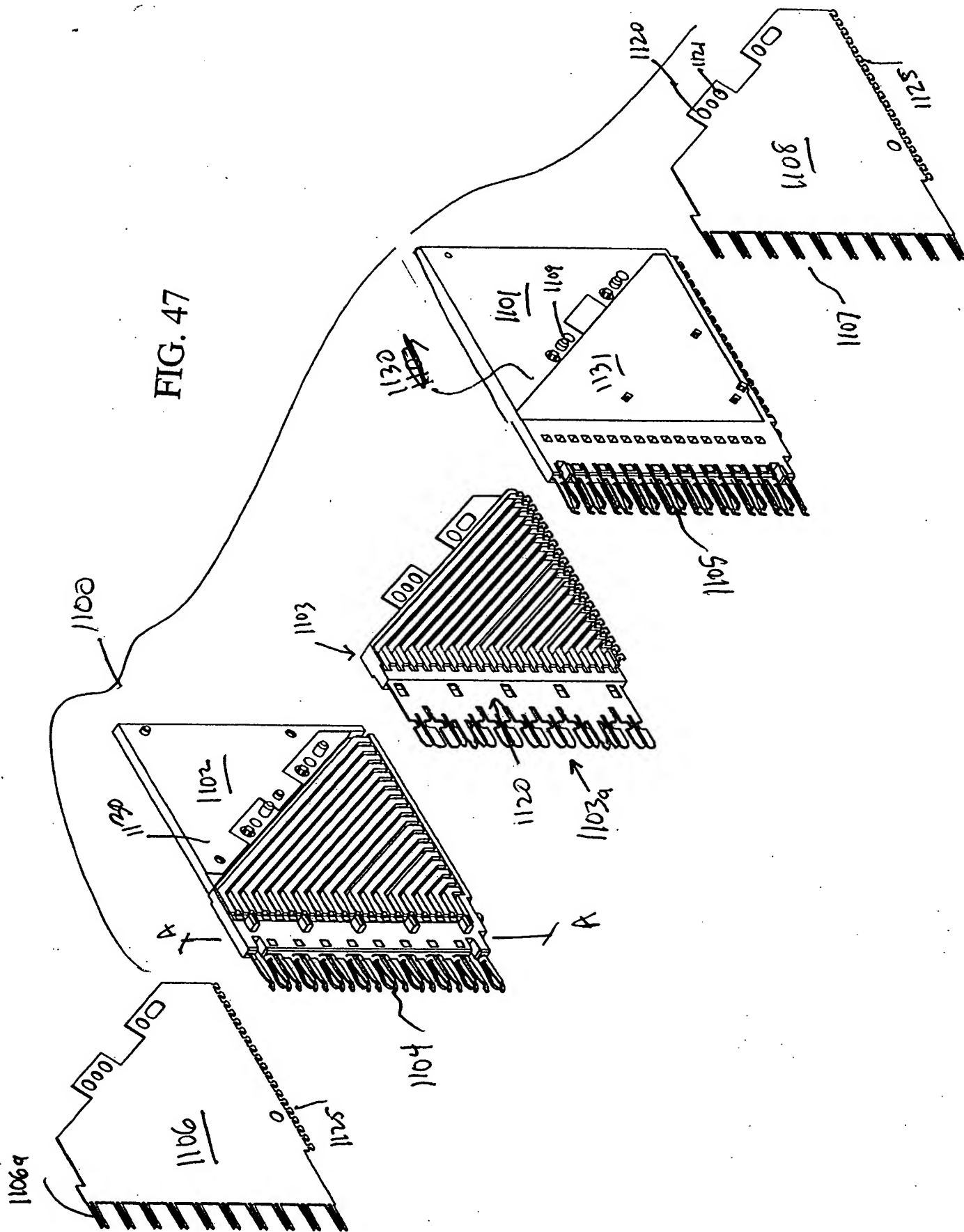


FIG. 47A

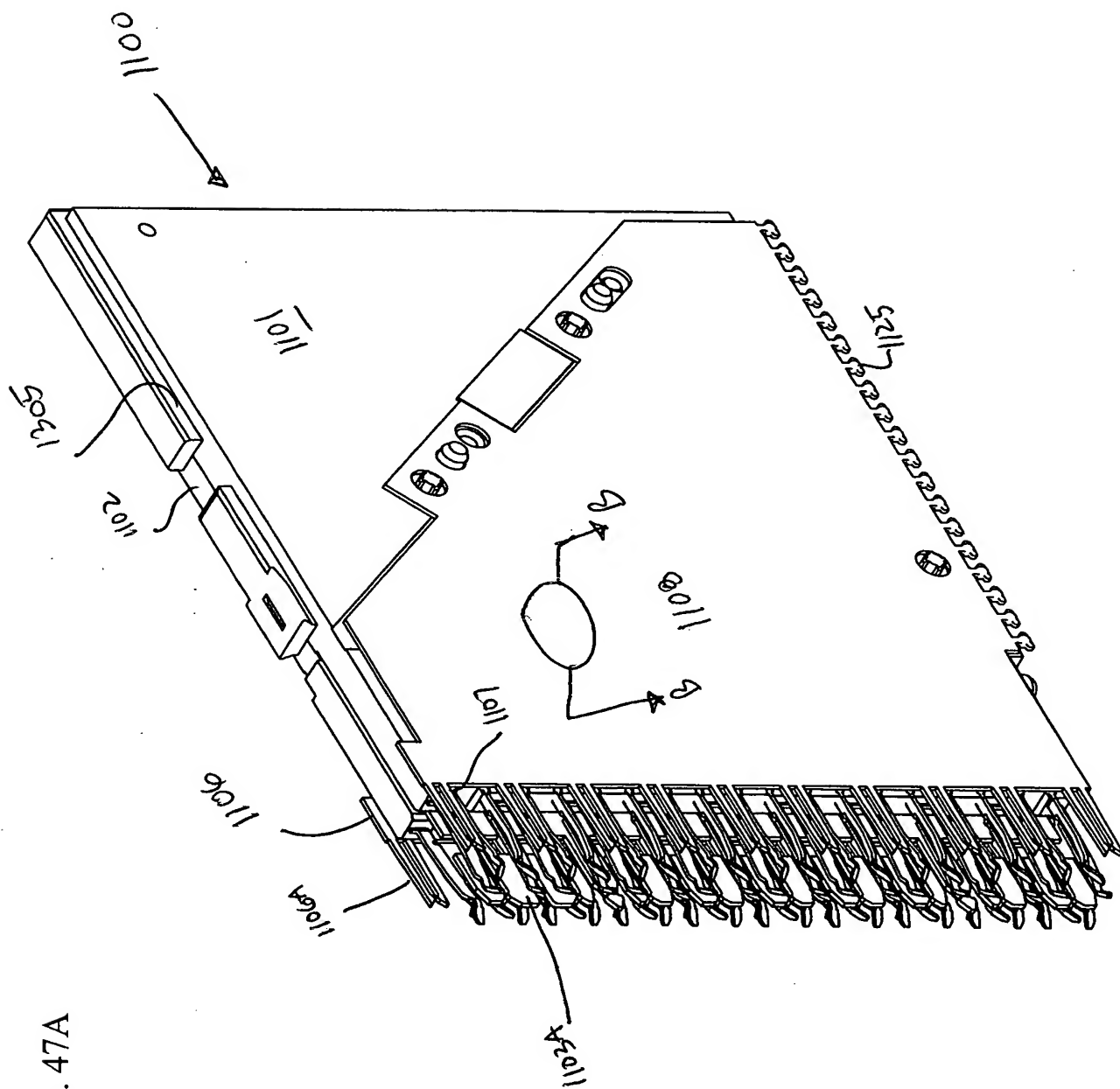


FIG. 48

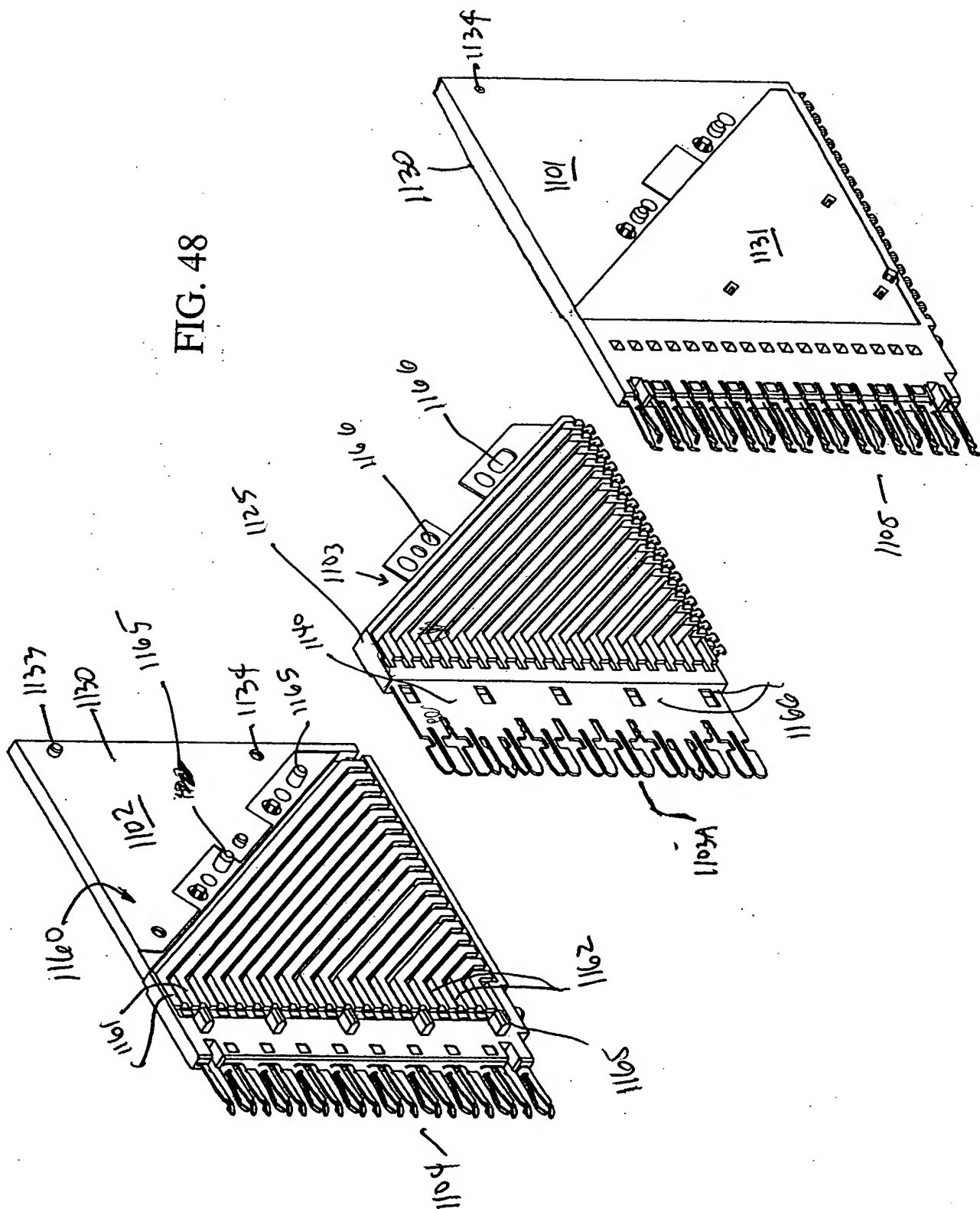


FIG. 48A

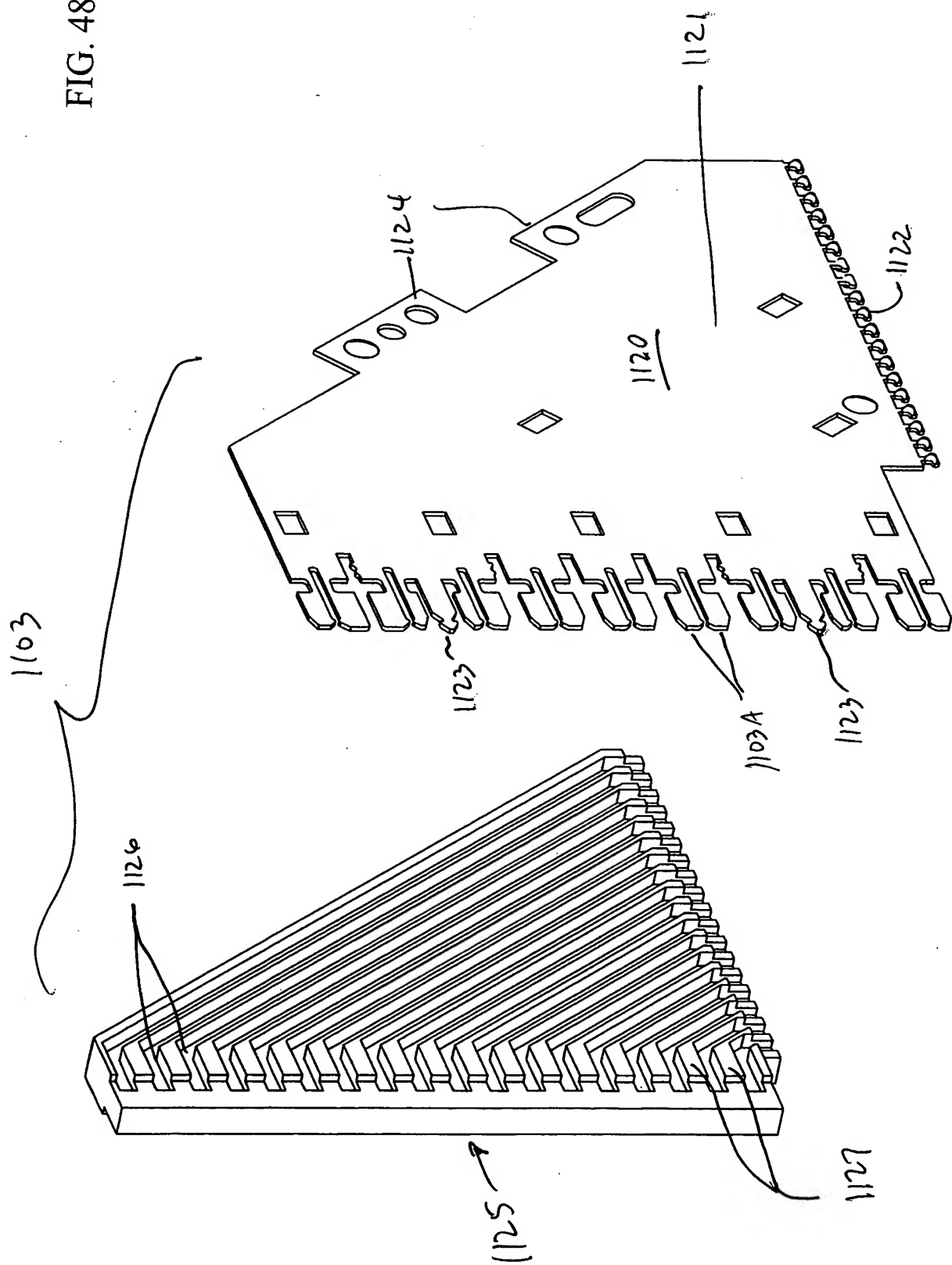




FIG. 49A

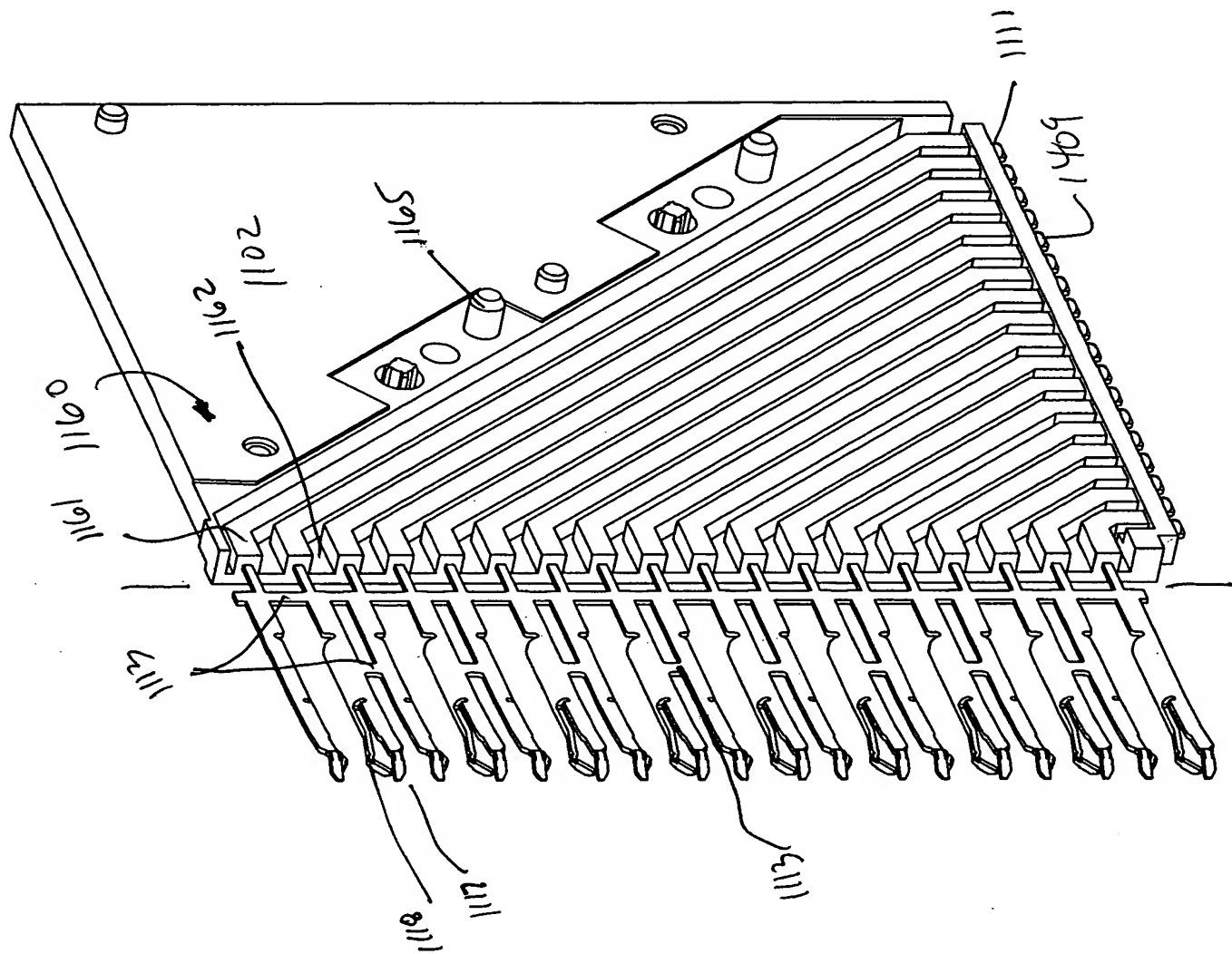


FIG. 50

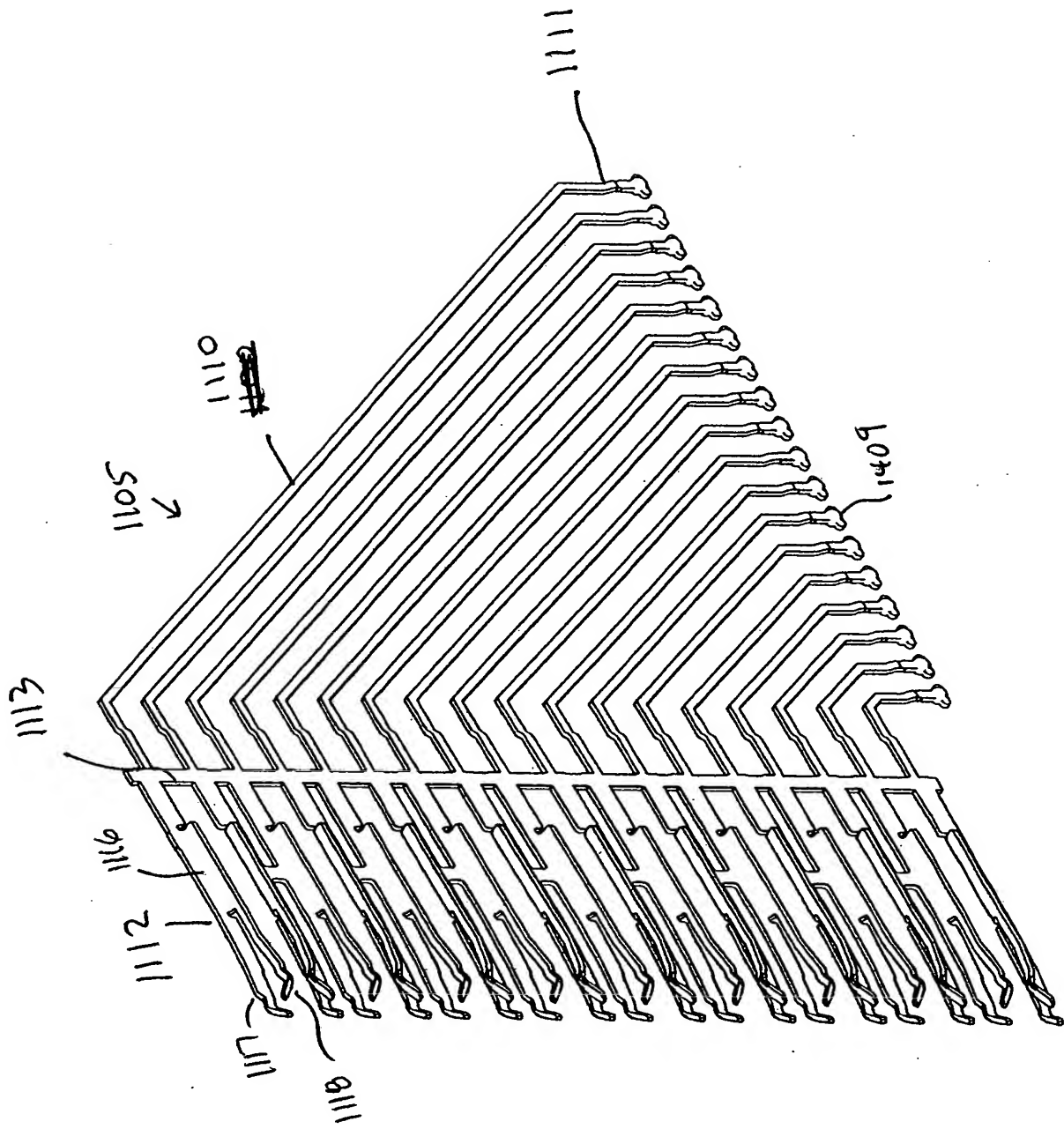


FIG. 51

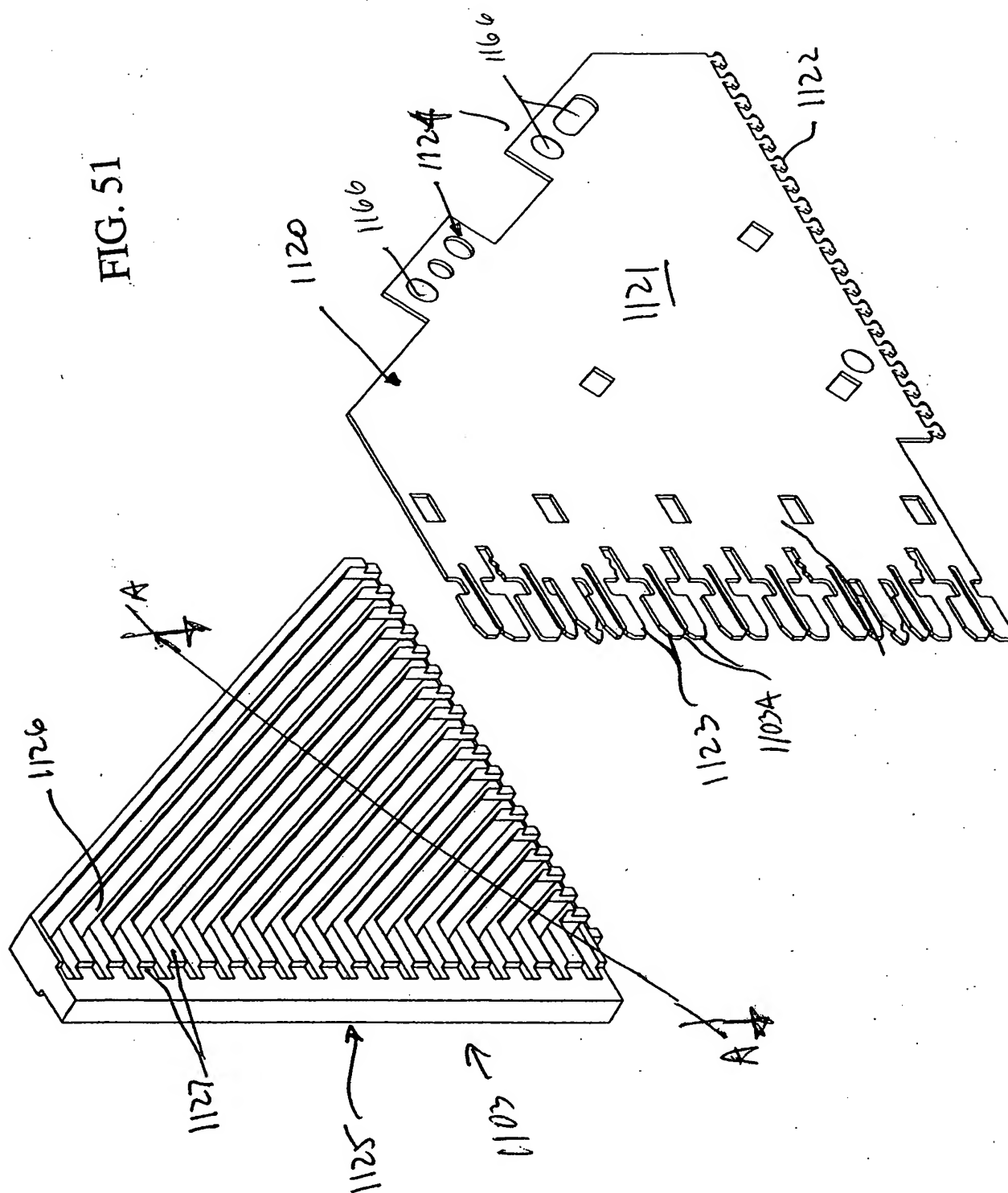




FIG. 51A

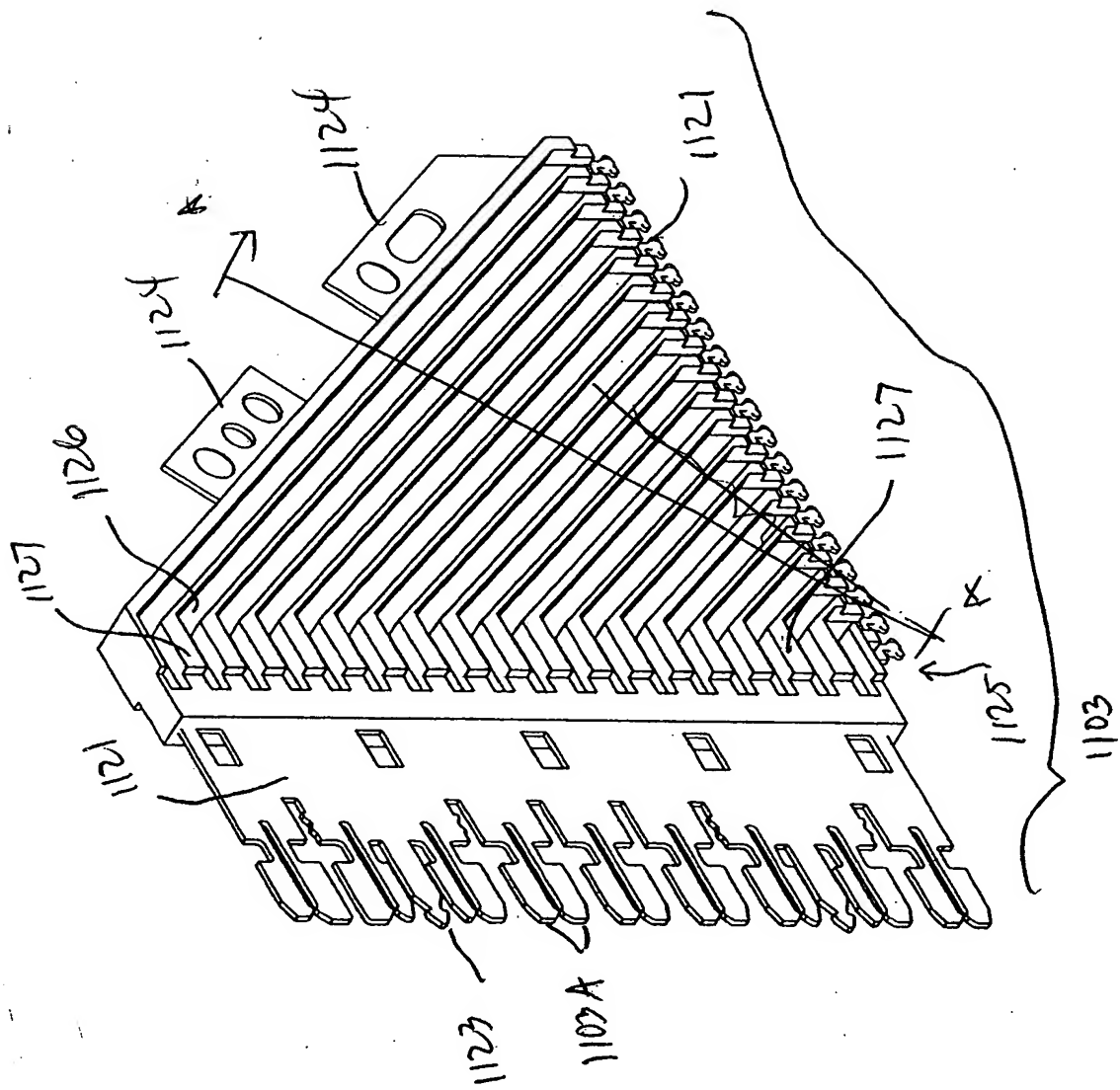


FIG. 52

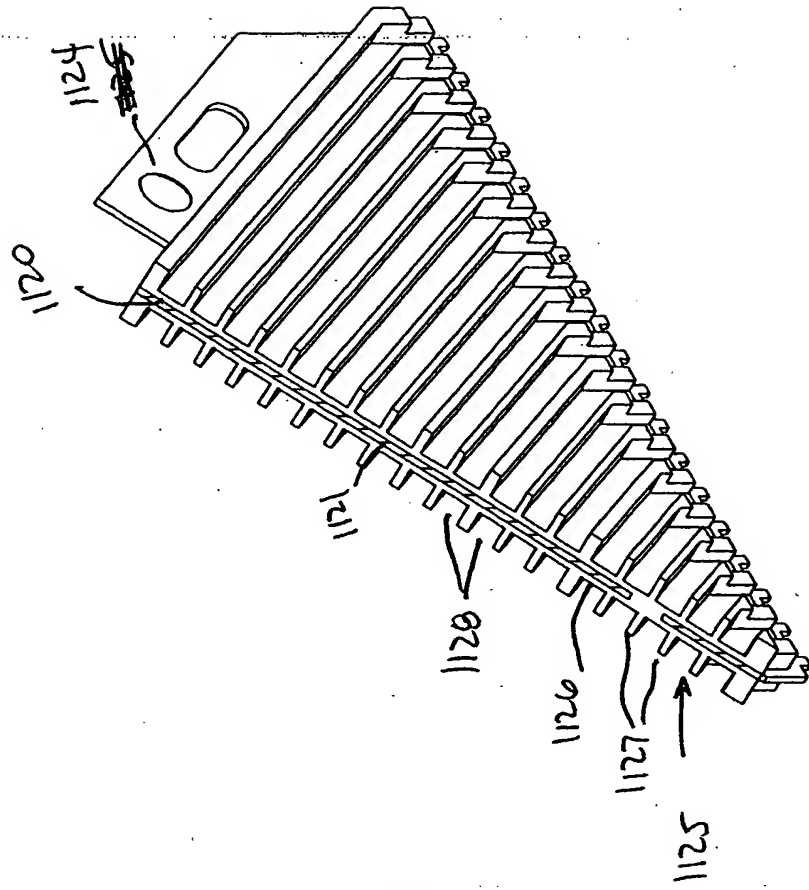


FIG. 53

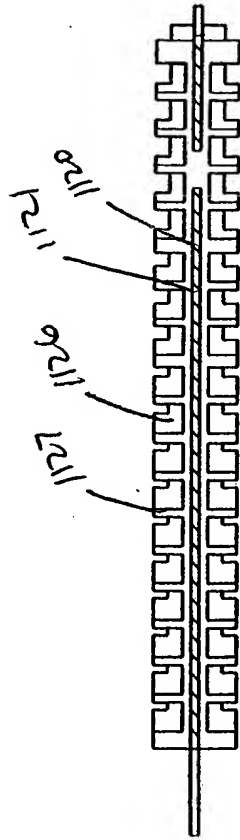


FIG. 54

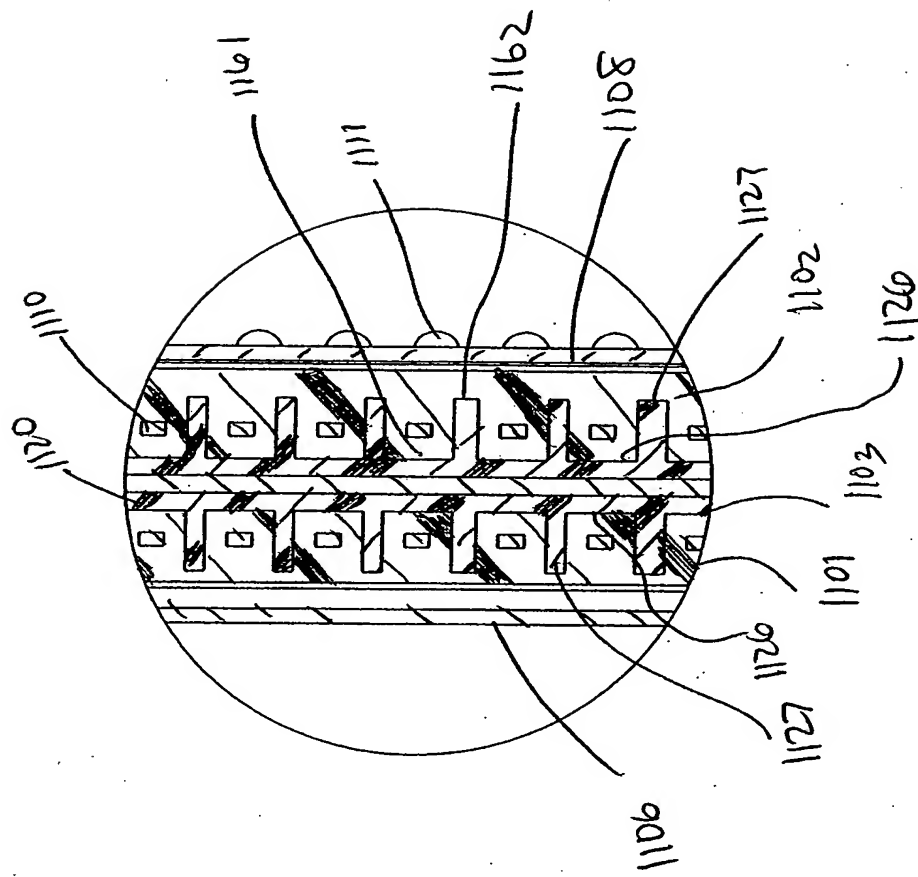


FIG. 55

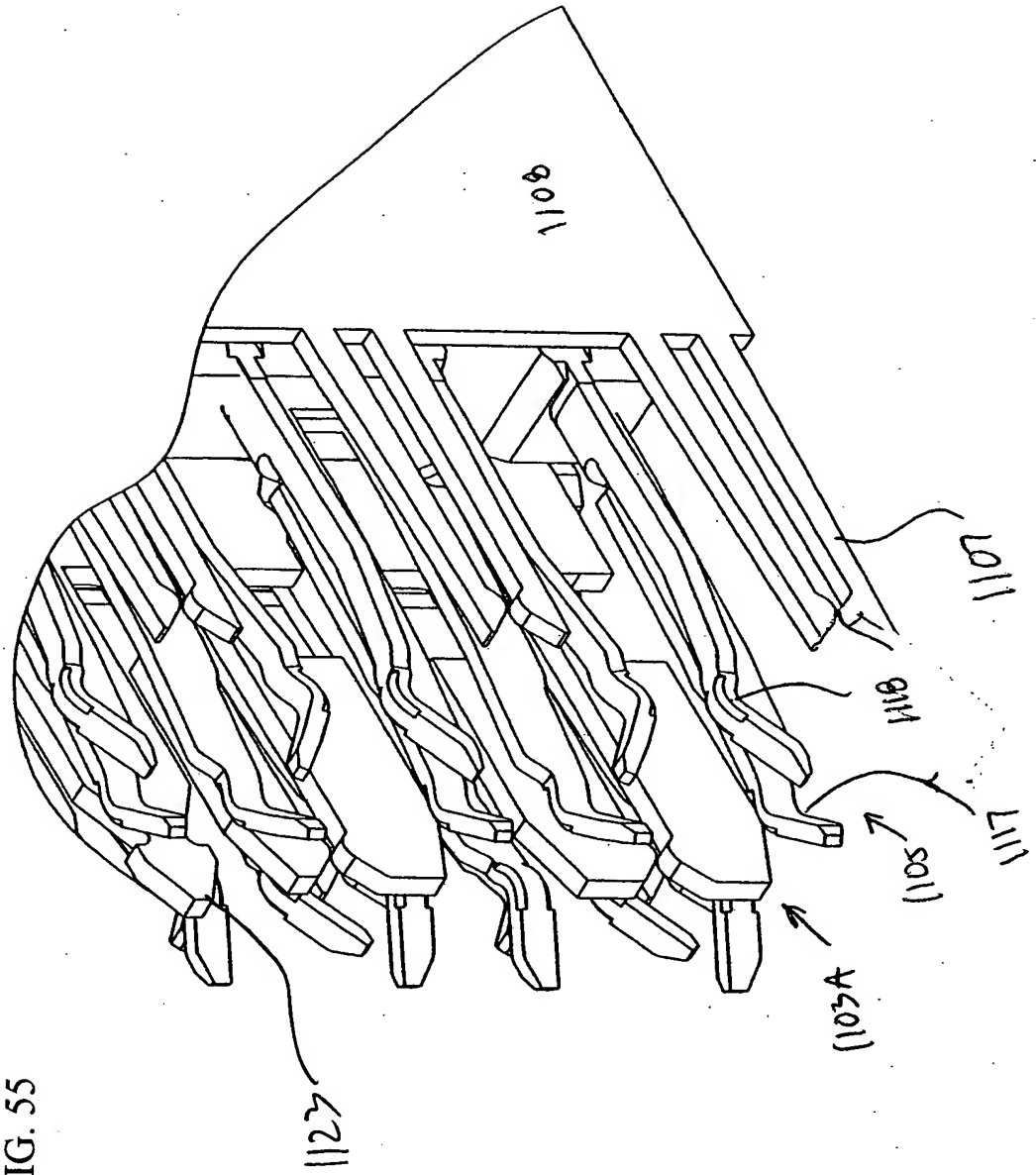


FIG. 56

